ECE 474a/574a: Computer-Aided Logic Design – Spring 2024

Time: Monday, Wednesday, Friday, 9am – 9.50am; Credits: 3
Location: Haury Anthropology Bldg, Rm 216
Global/Online Students Time: AOE (Videos will be posted to Panopto by 5pm on each class day.)
Prerequisites: ECE 275 (or **strong C++ programming skills**), ECE 274a, basic Linux commands (or access to Google)

Instructor

Tosiron Adegbija (https://tosiron.com), tosiron@arizona.edu
Office Hours: Fridays 4 – 5 pm (sign up before 3 pm; sign-up links on D2L and Piazza)
UA Global: Muhammad Bhakti (mbhakti@arizona.edu)

Course Websites

We will use Piazza (also accessible via *D2L -> Piazza*) for class resources, lecture notes, assignments, and discussion. The system is highly catered to getting you help fast and efficiently from classmates and myself. Unless you have questions specifically related to your grade, personal matters, or similar, you should post your questions to Piazza. Sign up link and access code are on D2L. All enrolled students *must* sign up on Piazza (**The sign-up code is given in the D2L class welcome message**).

If possible, I encourage you to post questions on Piazza *before* classes so that we can discuss the questions during class if necessary.

We will use D2L (https://d2l.arizona.edu) for Grades (via *D2L -> Grades*), assignment submission (via *D2L -> Assignments*), and class videos (posted after every class via *D2L -> Panopto*).

Course Overview

This course is an introduction to Computer-Aided Logic Design. This is a highly active research area, enabling the design of more complex digital systems. In this course we will focus on three areas: specification, optimization, and the use of software tools. The course will examine how to specify functionality at different abstractions, use industry-standard tools to synthesize and simulate hardware designs, and investigate some of the underlying optimization techniques utilized.

Topics include, but are not limited to:

- Hardware description languages (HDL)
- High-level synthesis (HLS): scheduling algorithms, resource sharing and binding, etc.
- Design and implementation of sequential circuits
- Register-transfer level (RTL) design
- Optimization and tradeoffs of combinational and sequential circuits
- Exact and heuristic minimization of two-level circuits

Learning Outcomes

By the end of this course, students will be able to:

- Understand the basics of high-level synthesis (HLS) and the benefits of HLS in improving productivity in the design of application-specific integrated circuits (or accelerators)

- Understand the importance of scheduling in HLS and learn how to use a variety of scheduling algorithms, including ASAP, ALAP, Hu, LIST_L, LIST_R, and force-directed
- Understand a variety of methods used for resource sharing and binding
- Understand the difference between heuristic and exact optimization methods, and be able to classify a variety of algorithms into these two categories
- Use advanced techniques for logic minimization, including the Quine-McCluskey tabular minimization technique for identifying all the prime implicants, and solve the covering problem using Petrick's method to find an optimal two-level implementation for specified logic functions
- Use Quine-McCluskey with iterative and recursive consensus methods for identifying the complete sum and solve the covering problem using row/column dominance to find a minimal gate, two-level implementation for specified logic functions
- Understand the role of verification in computer-aided design along with different testing methods
- Design a simple high-level synthesis tool in C/C++ to output the resulting Verilog circuit implementation, given a behavioral netlist specification

Textbooks

There is no required textbook. The class is designed so that you do not have to purchase any textbooks. However, the lecture notes are based on the following textbooks:

- Cormen, Leiserson, Rivest, and Stein, *Introduction to Algorithms,* Third Edition, MIT Press
- Frank Vahid and Roman Lysecky, *Verilog for Digital Design,* John Wiley & Sons
- Frank Vahid, *Digital Design,* John Wiley & Sons
- Robert K. Brayton, Gary D. Hatchel, C. McMullen, and Alberto L. Sangiovanni-Vincentelli, *Logic Minimization Algorithms for VLSI Synthesis,* Kluwer Academic Publishers
- Giovanni De Micheli, *Synthesis and Optimization of Digital Circuits,* McGraw-Hill

Communication with the Instructor

In general, questions about class contents should be posted on Piazza. That way, responses can be helpful to other students and other students (or the grader) may also be able to provide quicker responses to questions. Please be respectful in all your posts on Piazza, especially when answering other students' questions, even if the answers are obvious to you.

For questions related to grades and personal matters, please email me. In your emails to me, please **include the course number in brackets in your subject (i.e., [ECE 574A] or [ECE 474A])** so that I can sort my email and give a quicker response. **Please specify if you are an online or global student**.

Grading

The grading for the class will be performed on an individual basis. You will not be competing with other students for your grade. Your grade is only dependent on the effort you put into the class. Letter grades will be assigned using a 10% scale:

- 90 – 100%: A
- 80 – 89%: B
- 70 – 79% C
- 60 – 69% D

The grading will be based on a weighted sum as follows:

- 30% - Programming assignments (PA): 3 in total; each lasting about one month; group work
  - PA 1 involves using Verilog to implement different netlist descriptions and analyzing them using Xilinx Vivado synthesis (posted tentatively on *January 17,* due *Sunday, February 4*)
  - PA 2 involves using C or C++ to implement an HLS tool to convert a netlist description to the Verilog implementation (posted tentatively on *February 14,* due *Sunday, March 3*)
  - PA3 builds on PA2 to implement an HLS scheduling algorithm and generate a scheduled Verilog implementation of a netlist description (posted tentatively on *March 13*, due *Sunday, April 14*).
  - Assignments will feature additional components for ECE 574 students.
- 70% - Quizzes and exams
  - There will be several impromptu in-class or take-home quizzes and exams throughout the semester. For the take-home quizzes/exams, you are encouraged to attend class/watch the week's lecture videos before attempting the quizzes.
  - The weight of each individual quiz will be provided on each assignment. Most quizzes will be administered via the D2L Quiz function for all students.
- 3% - Class participation
  - To motivate participation in in-class and Piazza discussions, the top 10% of contributors on will receive a 3% bonus.

All grades will be posted on D2L.

Required Equipment and Software

- Reliable computer and Internet connection or access to computers in the ECE labs
- Free software:
  - Xilinx Vivado: You will need access to the free Webpack version of Xilinx Vivado
  - Your favorite C/C++ IDE
  - WinSCP or equivalent file transfer software

Policies

- ***No academic dishonesty will be tolerated. Unless otherwise instructed, all course work should be done on your own. Please consult the UA Code of Academic Integrity.***
- Students are expected to read any assigned material *before* lecture.
- No late work will be accepted, unless in extraordinary circumstances, e.g., medical emergency, University/College approved absences, etc.
- Missed exams and assignments can only be made up in case of documented illness or personal emergency. Please submit a written documentation (including supporting documentation) to me ASAP. When possible, make-up arrangements must be made prior to the scheduled activity.
- Even though I will not be taking roll, I highly recommend that you attend class sessions regularly and/or promptly watch lecture videos. I have seen a direct correlation of positive learning outcomes and good grades to consistent class attendance and active engagement with the classes.

Disability/Counseling Resources

At the University of Arizona, we strive to make learning experiences as accessible as possible. If you anticipate or experience barriers based on disability or pregnancy, please contact the Disability Resource Center (520-621-3268, https://drc.arizona.edu) to establish reasonable accommodations.

Additionally, resources are available on campus to students having personal problems or lacking clear career and academic goals. Students who need assistance should contact Counseling and Psych Services for the necessary assistance.

Inclusive Excellence

Inclusive Excellence is a fundamental part of the University of Arizona's strategic plan and culture. As part of this initiative, the institution embraces and practices diversity and inclusiveness. These values are expected, respected, and welcomed in this course.

This syllabus is subject to change at the discretion of the instructor, with proper notice to the students.