ECE 274A – Digital Logic
Spring 2016 (MWF 10:00-10:50AM, HARV 302)
http://www.ece.arizona.edu/~ece274

Instructor
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Textbooks
We are going to use the online version of the "Digital Design" textbook by Frank Vahid. Please follow these instructions for accessing the book:
1. Sign up at zyBooks.com
2. Enter zyBook code: ArizonaECE274ASpring2016
3. Click 'Subscribe'

The following books are recommended if you choose to have additional resources:
-Digital Design, 2nd edition, Frank Vahid, John Wiley and Sons
-Digital Design and Computer Architecture, David Harris, Sarah Harris, Morgan Kaufmann
-Contemporary Logic Design, Randy H. Katz, Gaetano Borriello, Prentice Hall
-Verilog for Digital Design, Frank Vahid, Roman Lysecky, John Wiley and Sons

Overall Educational Goal
We will cover fundamental digital design concepts in this class. You will learn how to design and implement basic building blocks of a digital system. You will then learn how to put together these pieces to construct digital components of larger systems such as a medical device, automobile, cell phone, home security system, robot, and many many other systems. This is going to be a challenging class, yet a very rewarding one for your future career.

Prerequisite: Programming in C/C++

Course outline
- Boolean Algebra,
- Combinational Logic, Common Combinational Components
- Basic Storage Elements
- Controllers, Sequential Logic Design Process
- Multifunction Registers, Adders, Incrementers, Comparators, Multipliers
- Subtractors, Signed Numbers, ALUs, Shifters, Counters, Timers, Register Files
- RTL Design
- Combinational Optimization, Sequential Optimizations
- Datapath Component Tradeoffs
- Physical Implementation, FPGA Overview

Course organization
- Course involves class (3 credits) and laboratory (1 credit) activities.
- Class activities will involve assignments, quizzes, design challenges, 4 examinations and a comprehensive final exam.

- Participation on Piazza (https://www.piazza.com) will constitute extra credit (1% of final grade)

General policies

- NO LATE ASSIGNMENTS WILL BE ACCEPTED, except under extreme non-academic circumstances discussed with me at least three days before the assignment is due.
- **Make-ups** for assignments and exams *may* be arranged if a student's absence is caused by documented illness or personal emergency. A written explanation (including supporting documentation) must be submitted to me. If the explanation is acceptable, an alternative to the graded activity will be arranged.
- **Regrade** requests must be submitted in writing within **three days** after the grades have been received/posted.
- Any extenuating circumstances that have an impact on your participation in the course should be discussed with me as soon as those circumstances are known.
- Inquiries about graded material have to be turned in within three days of receiving a grade.
- I reserve the right to modify course policies, course calendar, assignment values and due dates, as circumstances require.
- You are strongly encouraged to attend the classes. In general, I have found that positive learning outcomes and good grades are highly correlated with consistent class attendance and in-person interactions with instructors/TAs during class/office hours. Also, there will be material covered in class that may not be on the slides or in the textbook. Lecture notes are intended to serve as a supplement and not as a substitute for attending class.
- You are encouraged to discuss the assignment specifications with me, your teaching assistants, and your fellow students. However, anything you submit for grading must be unique and should NOT be a duplicate of another source. The Department of Electrical and Computer Engineering expects all students to adhere to UofA's policies and procedures on Code of Academic Integrity. http://web.arizona.edu/~studpubs/policies/cacaint.htm

Laboratory (@ECE301)

Laboratory involves hands-on and coordinated sequence of activities in which students incrementally design, develop and test components using modern synthesis tools and FPGA prototyping boards. Students leave the class with a complete understanding of digital design from theory to practice, and with industry-relevant skills in design, development, debugging and testing. Laboratory activities will accompany the topics covered in the lectures with hands on programming based assignments. Please note that you may need to (and are encouraged to) *work outside of the lab section* to complete all of your assignments.

A lab assignment may have a pre-lab (checked by TA at the beginning of lab session) and code-check/demo (at the end of lab session). You must additionally submit your Verilog files for each lab assignment to the designated D2L dropbox on the day the lab assignment is due. Note, the code submitted on D2L should be the same code demoed in lab. Students **must** work in a group of two. Graduate students are required to work on an individual basis.

In addition, students will complete a lab practical on an individual basis. Students will be provided with a short problem statement and have 75 minutes to design, test, and submit their solution and the accompanying testbench in the designated D2L drop box.

Grading

40% - Exams (4 total)
20% - Comprehensive final exam
25% - Lab Assignments (6-8 total) and Lab Practical (4 total)
15% - Reading and Participation Exercises (7%), Quizzes (8%) (in-class announced/pop)

Reading and Participation Exercises
After each lecture, a reading assignment will be given. Each reading assignment from the online book will involve participation exercises. Completing these exercises before the next class will be mandatory. Those exercises will be graded as your assignments. Weight of a participation assignment will be in the range of 2-10 points based on the amount of workload required by that assignment. Your progress in reading and participation exercises as of 9:30am on the due date will be used for grading by me and TAs online. There is no formal assignment submission.

Students with Disabilities
If you anticipate the need for reasonable accommodations to meet the requirements of this course, you must register with the Disability Resource Center and request that the DRC send me official notification of your accommodation needs as soon as possible. Please plan to meet with me by appointment or during office hours to discuss accommodations and how my course requirements and activities may impact your ability to fully participate.