Roman Lysecky

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University of Arizona
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RESEARCH INTERESTS

My current research interests focus on embedded systems, with emphasis on embedded system security, non-intrusive system observation methods for in-situ analysis of complex hardware and software behavior, runtime optimizations methods, and design methods safety-critical and mobile health systems.

EDUCATION

Ph.D. June 2005, Computer Science, University of California, Riverside
Dissertation: *Warp Processing and Just-in-Time Field Programmable Gate Array Compilation*.
Received Outstanding Dissertation Award, European Design and Automation Association (EDAA)

M.S. September 2000, Computer Science, University of California, Riverside
Thesis: *Pre-fetching for Improved Core Interfacing*.

B.S. June 1999, Computer Science, University of California, Riverside
Graduated Cum Laude, Outstanding Student in Computer Science, Outstanding Student in Engineering

RESEARCH & INDUSTRY EXPERIENCE

Professor, August 2018 – Present
Associate Professor, August 2011 – July 2017
Faculty Fellow, August 2015 – July 2016
Assistant Professor, August 2005 – August 2011
Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ

- Formal models and runtime methods for automated detection and mitigation of security and privacy threats in medical devices and life critical systems.
- Design of nonintrusive hardware-based methods for runtime security and verification of embedded systems.
- Development of novel models for side-channels attacks that are portable across different embedded systems architectures and can be constructed using simulation rather than physical device access.
- Self-adaptive systems capable of runtime adaptation to account for dynamically changing system inputs, performance or energy requirements, and unknown environment conditions. Self-adaptation methods can be utilized to improve performance, minimize energy consumption, or determine novel system compositions to meet dynamic changing and unpredictable systems requirements.
- Dynamic profiling, optimization, and adaptation of heterogeneous distributed embedded systems focused on application experts to design, configure, and optimize complex embedded systems.

VP of Technology Enabled Content, December 2018 – Present
Authoring Co-Lead, February 2013 – December 2018
Author, July 2012 – Present
zyBooks, A Wiley Brand, Campbell, CA

- Lead authoring of zyBooks (zybooks.com): web-native, interactive replacement for textbooks that incorporate extensive animations, interactive tools, learning questions sets, integrated development environments, auto-generated and auto-graded homework assignments, etc.
- Conduct research to evaluate the efficacy of zyBooks, with key results demonstrating increased student performance by more than 1/4 of a letter grade on average compared to traditional textbooks.
- Authored and contributed to zyBooks on *Programming in C, Programming in Java, Java Early Objects, AP Java, Programming in C++, Data Structures Essentials, Data Structures Essentials: Pseudocode with Python Examples, Data Structures Essentials: Pseudocode with Java Examples, Web Programming, Digital Design, Fundamentals Programming Concepts, Troubleshooting Basics, and Introduction to Computer Systems and Assembly Programming.*

Graduate Student Researcher, 2001 – 2005, 1998 – 2000
Department of Computer Science and Engineering, University of California, Riverside.

- Developed warp processors that dynamically and transparently optimize an executing software binary by moving software kernels to on-chip configurable logic, resulting in better performance and lower energy.
- Developed custom CAD-oriented configurable logic fabric and supporting lean on-chip computer-aided design (CAD) tools used within warp processors.

Hardware Engineer, July 2001 – August 2001
Morpho Technologies, Irvine, CA

- Extended a RISC processor core to reduce power consumption using guarded evaluations of internal components within the processor's datapath.
- Developed methodology for gate-level power analysis using back-annotated gate-level simulations for Cadence design tools to quickly evaluate the effects of architectural modifications on power consumption.

Software Engineer, August 2000 – July 2001
Conexant Inc., Newport Beach, CA

- Developed a web-enabled software engineering tool that dramatically improve human comprehension of large software projects and enabled efficient recovery of legacy software IP.

HONORS, AWARDS, AND ACHIEVEMENTS

- **Best Paper Award**, *Statistical Time-based Intrusion Detection in Embedded Systems*. IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2020.
- **Best Paper Award**, *Window-based Statistical Timing of Subcomponents for Efficient Detection of Malware in Life-Critical Systems*. Modeling and Simulation in Medicine, Spring Simulation Multi-conference (SpringSim), 2019
- **Best Paper Award**, *Composable Template Attacks using Templates for Individual Architectural Components*. International Conference on Computer Design (ICCD), 2018

- **Best Paper Award**, *Composite Risk Modeling for Automated Threat Mitigation in Medical Devices.* Modeling and Simulation in Medicine, Spring Simulation Multi-conference (SpringSim), 2017.
- **Best Paper Award**, *Student Performance Improvement using Interactive Textbooks: A Three-University Cross-Semester Analysis*. American Society for Engineering Education (ASEE) Annual Conference, 2015.
- **Best Paper Award**, *Hardware/Software Communication Middleware for Data Adaptable Embedded Systems*. IEEE International Conference on Engineering of Computer-Based Systems (ECBS), 2011.
- **Best Paper Award,** *A One-Shot Dynamic Optimization Methodology for Wireless Sensor Networks*. International Conference on Mobile Ubiquitous Computing, Systems, Services (UBICOMM), 2010.
- **Best Paper Award**, *Hardware/Software Partitioning of Floating Point Software Applications to Fixed-Pointed Coprocessor Circuits*, IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS), 2008.
- **Best Paper Award**, *Techniques for Reducing Read Latency in Core Bus Wrappers*, IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2000.
- **National Science Foundation,** Research featured in *Cardi-Hack* episode of "The Discovery Files", May 31, 2017.
- **6th Most Cited Article in ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Warp Processors, Compiled July 2015.
- **Senior Member**, Institute of Electrical and Electronics Engineers (IEEE), 2014.
- **Senior Member**, Association for Computing Machinery (ACM), 2014.
- **Excellence at the Student Interface**, College of Engineering, University of Arizona, 2013.
- **Excellence at the Student Interface**, College of Engineering, University of Arizona, 2008.
- **Outstanding Dissertation Award** for New Directions in Embedded System Design and Embedded Software, European Design and Automation Association (EDAA), 2007.
- **Outstanding Student in Computer Science**, University of California, Riverside, 1999.
- **Outstanding Student in Engineering**, University of California, Riverside, 1999.
- **GAANN (Graduate Assistance in Areas of National Need) Fellowship**, U.S. Dept. of Education at the University of California, Riverside, 1999 – 2000, 2001 – 2003.
- **Dean's Fellowship**, University of California, Riverside, 2001.
- **Chancellor's Fellowship**, University of California, Riverside, 1999.
- **UC Chancellor Scholarship**, University of California, Riverside, 1996 – 1997.

RESEARCH FUNDING

1. *Runtime Adaptive Risk Assessment and Automated Mitigation*. PI, TechLaunch Arizona, $35,661, December 2020 – June 2021.
2. *CIRCLES: Congestion Impact Reduction via CAV-in-the-loop Lagrangian Energy Smoothing*. Co-PI (UC Berkeley Lead with University of Arizona, Vanderbilt, Temple, Rutgers, and Tennessee DOT; Project PI: Alexandre M. Bayen, UC Berkeley; University of Arizona Lead: Jonathan Sprinkle). Department of Energy/Advanced Vehicle Technologies Research. $3,499,906 (University of Arizona: $875,000).
3. *Formal Models and Self-Adaptive Techniques to Automatically Mitigate Privacy and Security Threats in Life-Critical Systems*. PI, UA Global, $49,981, July 2018 – June 2019.

4. *TWC: Small: Time-Centric Modeling of Correct Behaviors for Efficient Non-Intrusive Runtime Detection of Unauthorized System Actions*. PI, National Science Foundation (NSF), CNS-1615890, $453,413, October 2016 – September 2019.
5. *CSR: Medium: Modeling and Synthesis for Application-Specific Systems-on-a-Chip*. Co-PI (PI Frank Vahid, UCR; Co-PI Tony Givargis, UCI), National Science Foundation (NSF), CNS-1563652, $1,000,000, August 2016 – July 2020.
6. *Theoretical Foundations, Modeling, and Exploration for Analyzing Power Obfuscation in Secure Embedded Systems*. PI, Army Research Office (ARO), W911NF-16-1-0130, $445,000, April 2016 – March 2019.
7. *CPS: Synergy: Collaborative Research: Control of Vehicular Traffic Flow Via Low Density Autonomous Vehicles*, PI (Original PI Jonathan Sprinkle is now at NSF), National Science Foundation (NSF), CPS-1446435, $280,000, January 2015 – December 2018.
8. *Data-Adaptable Modeling and Optimization for Runtime Adaptable Systems*. PI, Air Force Office of Scientific Research, $50,000, May 2015 – April 2016.
9. *Analysis of Side Channel Attacks and Power Obfuscation Methods for Embedded*. PI, Western Alliance to Expand Student Opportunities, Undergraduate Research Project, $2000, January 2016 – May 2016.
10. *CAREER: Dynamic and Autonomous Software-to-Hardware Translation for High-Performance and Low-Power Embedded Computing*. PI, National Science Foundation, CNS-0844565, $415,874, February 2009 – January 2015.
11. *REU Supplement for CAREER: Dynamic and Autonomous Software-to-Hardware Translation for High-Performance and Low-Power Embedded Computing*. PI, National Science Foundation, CNS-0844565, $32,000, January 2012 – January 2013, May 2013 – January 2015.
12. *Embedded Systems Security using Runtime Monitoring*. PI, Western Alliance to Expand Student Opportunities, Undergraduate Research Project, $4000, January 2015 – May 2015, August 2015 – December 2015.
13. *Embedded Systems Security using Hardware-based Runtime Monitoring*. PI, Western Alliance to Expand Student Opportunities, Undergraduate Research Project, $2000, August 2014 – December 2014.
14. *Hardware-based Methods Supporting Secure Embedded Systems*. PI, Western Alliance to Expand Student Opportunities, Undergraduate Research Project, $2000, January 2014 – May 2014.
15. *CSR: Small: Data-Adaptable Reconfigurable Embedded Systems (DARES)*. PI, National Science Foundation, CNS-0915010, $469,405, August 2009 – July 2013.
16. *Reducing Power Consumption of Sensor Based Systems Using Hardware DEVS Specification and Synthesis*. PI, Western Alliance to Expand Student Opportunities, Undergraduate Research Project, $5000, August 2012 – Dec 2012.
17. *Data-Adaptable Reconfigurable Embedded Systems (DARES)*. PI, Western Alliance to Expand Student Opportunities, Undergraduate Research Project, $5000, August 2011 – May 2012.
18. *Collaborative Research: CSR-EHCS, SM: DPOP – A Dynamic Profiling and Optimization Platform for Sensor-Based Networks*. Co-PI, National Science Foundation CNS-0834102, $200,000, August 2008 – July 2010.
19. *Asymmetric Threat Response and Analysis Program 3 (ATRAP 3)*. Co-PI. General Services Administration (US Army Battle Command Battle Lab), $2,079,808, September 2009 – September 2010.
20. *Non-intrusive Dynamic Instruction and Data Profiling for Soft Error Detection and Self-Healing Computing Systems*. PI, Toyota InfoTechnology Center, $54,623, February 2009.

21. *REU Supplement for Collaborative Research: CSR-EHCS, SM: DPOP – A Dynamic Profiling and Optimization Platform for Sensor-Based Networks*. Co-PI, National Science Foundation, CNS-0834102, $16,000, July 2009 – July 2010.
22. *Asymmetric Threat Response and Analysis Program 2 (ATRAP 2)*. Co-PI, General Services Administration (US Army Battle Command Battle Lab), $2,082,000, September 2008 – September 2009.
23. *Warp Processing Technology for Self-Healing Vehicle Electronic Circuit Applications*. PI, Toyota InfoTechnology Center, $45,000, March 2008.
24. *Asymmetric Threat Response and Analysis Program (ATRAP)*. Co-PI, General Services Administration (US Army Battle Command Battle Lab), $2,149,972, June 2007 – December 2008.

PATENTS

1. F. Vahid, R. Lysecky, G. Stitt. *Warp Processor for Dynamic Hardware/Software Partitioning*. US Patent 7,356,672, 2008.
2. R. Lysecky, J. Rozenblit, J. Sametinger, A. Rao, N. Carreon. *Runtime Adaptive Risk Assessment and Automated Mitigation*, Patent Application PCT/US19/59551.

PUBLICATIONS

Textbooks

1. R. Lysecky, F. Vahid, E. Olds. *Data Structures Essentials: Pseudocode with C++ Examples*. zyBooks, 2021.
2. R. Lysecky, F. Vahid, E. Olds. *Data Structures Essentials: Pseudocode with Java Examples*. zyBooks, 2020.
3. R. Lysecky, F. Vahid, E. Olds. *Data Structures Essentials: Pseudocode with Python Examples*. zyBooks, 2019.
4. F. Vahid, R. Lysecky. *Fundamental Programming Concepts*. zyBooks, 2018 – 2019.
5. F. Vahid, R. Lysecky. *Introduction to Computer Systems and Assembly Programming*. zyBooks, 2017, 2019.
6. F. Vahid, R. Lysecky. *Troubleshooting Basics*. zyBooks, 2016, 2018 – 2019.
7. F. Vahid, R. Lysecky, *Digital Design*, zyBooks, 2015, 2017 – 2018.
8. R. Lysecky, F. Vahid. *Data Structures Essentials*. zyBooks, 2013, 2015 – 2019.
9. R. Lysecky, A. Lizarraga. *Programming in Java*. zyBooks, 2013, 2015 – 2019.
10. R. Lysecky, A. Lizarraga. *Java Early Objects*. zyBooks, 2013, 2015 – 2019.
11. R. Lysecky, A. Lizarraga. *AP Java*. zyBooks, 2013, 2015 – 2019.
12. R. Lysecky, F. Vahid. *Programming in C*. zyBooks, 2012–2013, 2015 – 2019.
13. F. Vahid, R. Lysecky. *Programming in C++*. zyBooks, 2012–2013, 2015 – 2019.
14. F. Vahid, R. Lysecky. *VHDL for Digital Design*, John Wiley and Sons, 2007.
15. F. Vahid, R. Lysecky. *Verilog for Digital Design*, John Wiley and Sons, 2007.

Book Chapters

1. R. Lysecky (Senior Contributor). *Web Programming*, zyBooks, 2016 – 2018.

2. G.D. Burd, D. Tomanek, P. Blowers, M. Bolger, J. Cox, L. Elfring, E. Grubbs, J. Hunter, K. Johns, L. Lazos, R. Lysecky, J.A. Milsom, I. Novodvorsky, J. Pollard, E. Prather, V. Talanquer, K. Thamvichai, H. Tharp, C. Wallace. *Developing Faculty Cultures for Evidence-Based Teaching Practices in STEM: A Progress Report*. In *Transforming Institutions, Undergraduate STEM Education for the 21st Century*, Purdue University Press, pp. 90-102, 2015.
3. R. Lysecky, K. Shankar. *Methods for Non-Intrusive Dynamic Application Profiling and Soft Error Detection*. In *Embedded and Networking Systems Design, Software, and Implementation*, Chapman and Hall/CRC, 2013.
4. A. Gordon-Ross, S. Lysecky, R. Lysecky, A. Munir, A. Shenoy, J. Hiner. *Dynamic Profiling and Optimization Methodologies for Sensor Networks*, In *Building Sensor Networks from Design to Applications*, CRC Press, 2013.
5. R. Lysecky (Co-author). *Hardware Description Languages*. In *Digital Design*, John Wiley and Sons, 2006.

Journal Papers

1. G. Gunter, D. Gloudemans, R. Stern, S. McQuade, R. Bhadani, M. Bunting, M. L. Delle Monache, R. Lysecky, B. Seibold, J. Sprinkle, B. Piccoli, D. Work. *Are commercially implemented adaptive cruise control systems string stable?* Transactions on Intelligent Transportation Systems, *Accepted*, 2020.
2. N. Carreon, S. Lu, R. Lysecky. *Probabilistic Estimation of Threat Intrusion in Embedded Systems for Runtime Detection*. ACM Transactions on Embedded Computing Systems (TECS), Vol. 20, No. 2, Article 14, 27 pages, 2021.
3. C. Bresch, D. Hely, S. Chollet, R. Lysecky. *SecPump: A Connected Open Source Infusion Pump for Security Research Purposes.* IEEE Embedded Systems Letters (ESL), Vol. 13, No. 1, pp. 21-24, 2021.
4. C. Bresch, D. Hely, S. Chollet, R. Lysecky, I. Parissis. *TrustFlow-X: A Practical Framework for Fine-Grained Control-Flow Integrity in Critical Systems*. ACM Transactions on Embedded Computing Systems (TECS), 19(5), Article 36, 26 pages, 2020.
5. F. Vahid, T. Givargis and R. Lysecky. *A Pattern Recognition Framework for Embedded Systems*. The American Society for Engineering Education (ASEE) Computers in Education (CoED) Journal, Vol. 11, No. 1, 13 pages, 2020.
6. A. Lizarraga, J. Sprinkle, R. Lysecky. *Automated Model-based Optimization of Data- Adaptable Embedded Systems*. ACM Transactions on Embedded Computing Systems (TECS), 19(1), Article 8, 22 pages, 2020.
7. H. Nam, R. Lysecky. *Security-Aware Multi-Objective Optimization of Distributed Reconfigurable Embedded Systems*. Journal of Parallel and Distributed Computing, Volume 133, November 2019, Pages 377-390, 2019.
8. S. Lu, R. Lysecky. *Data-driven Anomaly Detection with Timing Features for Embedded Systems*. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 24, No. 3, Article 33, 27 pages, 2019.
9. M. Seo, R. Lysecky. *Non-Intrusive In-Situ Requirements Monitoring of Embedded System*. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 23, No. 5, Article 58, 27 pages, 2018.
10. H. Nam, R. Lysecky. *Mixed Cryptography Constrained Optimization for Heterogeneous, Multicore, and Distributed Embedded Systems*. Computers, 7(2), 29, 2018.
11. A. Rao, N. Carreón, R. Lysecky, J. Rozenblit. *Probabilistic Security Threat Detection for Risk Management in Cyber-physical Medical Systems*, IEEE Software, Vol. 35, No. 1, pp. 38-43, January/February 2018.

12. S. Lu, R. Lysecky. *Time and Sequence Integrated Runtime Anomaly Detection for Embedded Systems*, ACM Transactions on Embedded Computing Systems (TECS), Vol. 17, No. 2, Article 38, 27 pages, 2017.

13. N. Sandoval, C. Mackin, S. Whitsitt, V. S. Gopinath, S. Mahadevan, A. Milakovich, K. Merry, J. Sprinkle, R. Lysecky. *Task Transition Scheduling for Data-Adaptable Systems*. ACM Transactions on Embedded Computing Systems (TECS), Vol. 16, No. 4, Article 105, 28 pages, 2017.

14. M. Seo and R. Lysecky. *In-Situ Requirements Monitoring of Embedded Systems*. IEEE Embedded Systems Letters (ESL), Vol. 8, No. 3, pp. 49-52, 2016.

15. J. C. Lee and R. Lysecky. *System-Level Observation Framework for Non-Intrusive Runtime Monitoring of Embedded Systems*. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 20, No. 3, pp. 1-27, 2015.

16. J. Sametinger, J. Rozenblit, R. Lysecky, P. Ott. *Security Challenges for Medical Devices*. Communication of ACM (CACM), Vol. 58 No. 4, Pages 74-82, 2015.

17. L. Ding, A. Lizarraga, A. Shenoy, A. Gordon-Ross, S. Lysecky, R. Lysecky. *Application-Specific Customization of Dynamic Profiling Mechanisms for Sensor Networks*. IEEE Access, Vol. 3, pp. 303-322, 2015.

18. J. C. Lee, J. Vance, and R. Lysecky. *Hardware-based Event Stream Ordering for System-level Observation Framework*. IEEE Embedded Systems Letters (ESL), Vol. 6, No. 4, pp. 81-84, 2014.

19. J. Sun, R. Lysecky, K. Shankar, A. Kodi, A. Louri, J. Roveda. *Workload Assignment* Considering NBTI Degradation in Multi-core Systems, ACM Journal on Emerging Technologies in Computing Systems (JETC), Vol. 10, No. 1, Article 4, pp. 1-22, 2014.

20. A. Lizarraga, R. Lysecky, S. Lysecky, A. Gordon-Ross. *Dynamic Profiling and Fuzzy Logic Based Optimization of Sensor Networks Platforms*. ACM Transactions on Embedded Computing Systems (TECS), Vol. 13, No. 3, Article 51, pp. 1-29, 2013.

21. J. Mu, K. Shankar, R. Lysecky. *Profiling and Online System-Level Performance and Power Estimation for Dynamically Adaptable Embedded Systems*. ACM Transactions on Embedded Computing Systems (TECS), Vol. 12, No. 3, Article 85, pp. 1-20, 2013.

22. A. Munir, A. Gordon-Ross, S. Lysecky, R. Lysecky. *A Lightweight Dynamic Optimization Methodology and Application Metrics Estimation Model for Wireless Sensor Networks*. Sustainable Computing, Informatics and Systems (SUSCOM), Vol. 3, No. 2, pp. 94–108, 2013.

23. A. Lizarraga, L. Ding, J. Hiner, R. Lysecky, S. Lysecky, A. Gordon-Ross. *ATLeS-SN A Modular Simulator for Wireless Sensor Networks*. Design Automation for Embedded Systems (DAEM), Vol. 16, No. 4, pp. 265-291, 2012.

24. J. Sun, R. Zheng, J. Velamala, Y. Cao, R. Lysecky, K. Shankar, J. Roveda. *A Self-tuning Design Methodology for Power-efficient Multi-core Systems*. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 18, No. 1, Article 4, pp. 1-24, 2012.

25. A. Munir, A. Gordon-Ross, S. Lysecky, R. Lysecky. *A One-Shot Dynamic Optimization Methodology and Application Metrics Estimation Model for Wireless Sensor Networks*. IARIA International Journal on Advances in Networks and Services (IJANS), Vol. 4, No. 3 & 4, pp. 278-291, 2012.

26. A. Nair, K. Shankar, R. Lysecky. *Efficient Hardware-Based Non-Intrusive Dynamic Application Profiling*. ACM Transactions on Embedded Computing Systems (TECS), Vol. 10, No. 3, Article 32, pp. 1-22, 2011.

27. K. Shankar, R. Lysecky. *Control Focused Soft Error Detection for Embedded Applications*, IEEE Embedded Systems Letters (ESL), Vol. 2, No. 4, pp. 127-130, 2010.

28. A. Shenoy, J. Hiner, S. Lysecky, R. Lysecky, A. Gordon-Ross. *Evaluation of Dynamic Profiling Methodologies for Optimization of Sensor Networks*. IEEE Embedded Systems Letters, Vol. 2, No. 1, pp. 10-13, 2010.
29. R. Kalra, R. Lysecky. *Configuration Locking and Schedulability Evaluation for Reduced Reconfiguration Overheads of Reconfigurable Systems*. IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 18, No. 4, pp. 67167-4, 2010.
30. J. Mu, R. Lysecky. *Autonomous Hardware/Software Partitioning and Voltage/Frequency Scaling for Low-Power Embedded Systems*. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 15, No. 1, Article 2, pp. 1-20, 2009.
31. L. Saldanha, R. Lysecky. *Float-to-Fixed and Fixed-to-Float Hardware Converters for Rapid Hardware/Software Partitioning of Floating Point Software Applications to Static and Dynamic Fixed Point Coprocessors*. Journal on Design Automation of Embedded Systems, Vol. 13, No. 3, pp. 139-157, 2009.
32. R. Lysecky, F. Vahid. *Design and Implementation of a MicroBlaze-based Warp Processor*. ACM Transactions on Embedded Computing Systems (TECS), Vol. 8, No. 3, Article 22, pp. 1-22, 2009.
33. R. Lysecky. *Scalability and Parallel Execution of Warp Processing - Dynamic Hardware/Software Partitioning*. International Journal on Parallel Processing, Vol. 36, No. 5, pp. 478-492, October 2008.
34. F. Vahid, G. Stitt, R. Lysecky. *Warp Processing: Dynamic Translation of Binaries to FPGA Circuits*. IEEE Computer, Vol. 41, No. 7, pp. 40-46, July 2008.
35. R. Lysecky, G. Stitt, F. Vahid. *Warp Processors*. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 11, No. 3, pp. 659 - 681, 2006. **6th Most Cited Article in ACM TODAES as of July 2015.**
36. C. Zhang, F. Vahid, R. Lysecky. *A Self-Tuning Cache Architecture for Embedded Systems*. ACM Transactions on Embedded Computing Systems (TECS), Vol. 3, No. 2, pp. 407-425, May 2004.
37. R. Lysecky, S. Cotterell, F. Vahid. *A Fast On-Chip Profiler Memory using a Pipelined Binary Tree*. IEEE Transaction on Very Large Scale Integration (TVLSI), Vol. 12, No. 1, pp. 120-122, January 2004.
38. F. Vahid, R. Lysecky, C. Zhang, G. Stitt. *Highly Configurable Platforms for Embedded Computing Systems*. Microelectronics Journal, Vol. 34, No. 11, pp. 1025-1029, 2003.
39. R. Lysecky, F. Vahid. *Pre-fetching for Improved Bus Wrapper Performance in Cores*. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 7, No. 1, pp. 58-90, January 2002.

Conference & Workshop Papers

1. F. Vahid, J. Allen, A. Edgcomb, R. Lysecky. *Using the free Coral language and simulator to simplify first-year programming courses*. ASEE First-Year Engineering Conference (FYEE), 2020.
2. D. McKinney, A. Edgcomb, R. Lysecky, F. Vahid. *Improving Pass Rates by Switching from a Passive to an Active Learning Textbook in CS0*. ASEE Annual Conference, 2020.
3. N. Carreón, A. Gilbreath, R. Lysecky. *Statistical Time-based Intrusion Detection in Embedded Systems*. IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2020. **Received Best Paper Award**
4. C. Bresch, D. Hely, R. Lysecky. *BackFlow: Backward Edge Control Flow Enforcement for Low End ARM Microcontrollers*. IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2020.
5. F. Vahid, A. Edgcomb, R. Lysecky, Y. Rajasekhar. *New web-based learning content for core programming concepts using Coral*. IEEE Frontiers in Education (FIE), 2019.

6. A. Rao, N. Carreón, R. Lysecky, J. Rozenblit, J. Sametinger. *Resilient Security of Medical Cyber-physical Systems*. International Workshop on Cyber-Security and Functional Safety in Cyber-Physical Systems (IWCPS), 2019.
7. A. Edgcomb, F. Vahid, R. Lysecky. *Coral: An Ultra-Simple Language for Learning to Program*. ASEE Annual Conference, 2019.
8. T. Adegbija, R. Lysecky, V. V. Kumar. *Right-Provisioned IoT Edge Computing: An Overview*. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2019.
9. M. Seo, R. Lysecky. *Automatic Extraction of Requirements from State-based Hardware Designs for Runtime Verification*. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2019.
10. N. Rascon, A. Gilbreath, R. Lysecky. *Window-based Statistical Timing of Subcomponents for Efficient Detection of Malware in Life-Critical Systems*. Modeling and Simulation in Medicine (MSM), Spring Simulation Multi-conference (SpringSim), 2019. **Received Best Paper Award**
11. G. Gunter, Y. Wang, D. Gloudemans, R. Stern, D. Work, M.L.D Monache, R. Bhadani, M. Bunting, R. Lysecky, J. Sprinkle, B. Seibold, B. Piccoli. *WiP Abstract: String stability of commercial adaptive cruise control vehicles*. ACM/IEEE International Conference on Cyber Physical Systems (ICCPS), 2019.
12. B. Liu, R. Lysecky, J. Roveda. *Composable Template Attacks using Templates for Individual Architectural Components*. International Conference on Computer Design (ICCD), 2018. **Received Best Paper Award**
13. N. Carreon, S. Lu, R. Lysecky. *Hardware-based Probabilistic Threat Detection and Estimation for Embedded Systems*. International Conference on Computer Design (ICCD), 2018.
14. M. Seo, R. Lysecky. *Work in Progress: Runtime Requirements Monitoring for State-based Hardware*. International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS), 2018.
15. N. Alzahrani, F. Vahid, A. Edgcomb, R. Lysecky, S. Lysecky. *An Analysis of Common Errors Leading to Excessive Student Struggle on Homework Problems in an Introductory Programming Course*. ASEE Annual Conference, 2018.
16. B. Liu, K. Chen, M. Seo, J. Roveda, R. Lysecky. *Evaluation of the Complexity of Automated Trace Alignment using Novel Power Obfuscation Methods*, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2018.
17. A. Rao, J. Rozenblit, R. Lysecky, J. Sametinger. *Trustworthy multi-modal framework for life-critical systems security*. Annual Simulation Symposium (ANSS). Spring Simulation Multi-conference (SpringSim), Article 17, 9 pages, 2018.
18. N. Alzahrani, F. Vahid, A. Edgcomb, K. Nguyen, R. Lysecky. *Python Versus C++: An Analysis of Student Struggle on Small Coding Exercises in Introductory Programming Courses*. ACM Technical Symposium on Computer Science Education (SIGCSE), 2018.
19. R. Lysecky, F. Vahid. *Teaching Students a Systematic Approach to Debugging*. ACM Technical Symposium on Computer Science Education (SIGCSE), 2018.
20. S. Lu, R. Lysecky, J. Rozenblit. *Subcomponent Timing-based Detection of Malware in Embedded Systems*, International Conference on Computer Design (ICCD), 2017.
21. M. Seo, R. Lysecky. *Hierarchical Non-Intrusive In-Situ Requirements Monitoring for Embedded Systems*, International Conference on Runtime Verification, 2017.
22. S. Lu, L. Lazos, R. Lysecky. *FEAL: Fine-Grained Evaluation of Active Learning in Collaborative Learning Spaces*. ASEE Annual Conference, 2017.
23. A. Edgcomb, F. Vahid, R. Lysecky, S. Lysecky. *An Analysis of Incorporating Small Coding Exercises as Homework in Introductory Programming Courses*. ASEE Annual Conference, 2017.

24. A. Rao, J. Rozenblit, R. Lysecky, J. Sametinger. *Composite Risk Modeling for Automated Threat Mitigation in Medical Devices*. Modeling and Simulation in Medicine, Spring Simulation Multi-conference (SpringSim), 2017. **Received Best Paper Award**
25. A. Edgcomb, F. Vahid, R. Lysecky, S. Lysecky. *Getting students to earnestly do reading, studying, and homework in an introductory programming class*. ACM Technical Symposium on Computer Science Education (SIGCSE), 2017.
26. S. Sargur, R. Lysecky. *Non-Intrusive Dynamic Profiler for Multicore Embedded Systems*. Asia and South Pacific Design Automation Conference (ASP-DAC), 2017.
27. A. Lizarraga, R. Lysecky, J. Sprinkle. *Model-based Fuzzy Logic Classifier Synthesis for Optimization of Data-Adaptable Embedded Systems*. International Conference on InfoSymbiotics/DDDAS, 2016.
28. F. Vahid, A. Edgcomb, S. Lysecky, R. Lysecky. *New Web-Based Interactive Learning Material for Digital Design*. ASEE Annual Conference, 2016.
29. A. Lizarraga, J. Sprinkle, R. Lysecky. *Model-driven Optimization of Data-Adaptable Embedded Systems*. IEEE Computer Software and Applications Conference (COMPSAC), 2016.
30. Hyunsuk Nam, R. Lysecky. *Latency, Power, and Security Optimization in Distributed Reconfigurable Embedded Systems*. Reconfigurable Architecture Workshop (RAW), 2016.
31. A. Edgcomb, F. Vahid, R. Lysecky. *Students Learn More with Less Text that Covers the Same Core Topics*. IEEE Frontiers in Education (FIE), 2015.
32. F. Vahid, D. de Haas, S. Strawn, A. Edgcomb, S. Lysecky, R. Lysecky. *A Continual Improvement Paradigm for Modern Online Textbooks*. International Conference of Education, Research and Innovation (ICERI), 2015.
33. A. Edgcomb, D. De Haas, R. Lysecky, F. Vahid. *Student Usage and Behavioral Patterns with Online Interactive Textbook Materials*. International Conference of Education, Research and Innovation (ICERI), 2015.
34. S. Lu, R. Lysecky. *Analysis of Control Flow Events for Timing-based Runtime Anomaly Detection*. Workshop on Embedded System Security (WESS), 2015.
35. A. Edgcomb, F. Vahid, R. Lysecky, A. Knoesen, R. Amirtharajah, M. L. Dorf. *Student Performance Improvement using Interactive Textbooks: A Three-University Cross-Semester Analysis*. ASEE Annual Conference, 2015. **Received Best Paper Award**
36. S. Lu, M. Seo, and R. Lysecky. *Timing-based Anomaly Detection in Embedded Systems*. Asia South Pacific Design Automation Conference (ASP-DAC), pp. 809-814, 2015.
37. S. Whitsitt, J. Sprinkle, R. Lysecky. *Generating Model Transformations for Mending Dynamic Constraint Violations in Cyber Physical Systems*. Workshop on Domain-Specific Modeling (DSM), 2014.
38. J. C. Lee, R. Lysecky. *Area-Efficient Event Stream Ordering for Runtime Observability of Embedded Systems*. IEEE/ACM Design Automation Conference (DAC), Article 130, pp. 1-6, 2014.
39. T. Pifer, D. Schwartz, R. Lysecky, C. Seo, B. Zeigler. *Discrete Event System Specification, Synthesis, and Optimization of Low-Power FPGA-based Embedded Systems*. International Conference on Field-Programmable Technology (ICFPT), pp. 98-105, 2013.
40. N. Sandoval, C. Mackin, S. Whitsitt, R. Lysecky, J. Sprinkle. *Runtime Hardware/Software Task Transition Scheduling for Runtime-Adaptable Embedded Systems*. International Conference on Field-Programmable Technology (ICFPT), pp. 342-345, 2013.
41. R. Lysecky, N. Sandoval, S. Whitsitt, C. Mackin, J. Sprinkle. *Efficient Reconfiguration Methods to Enable Rapid Deployment of Runtime Reconfigurable Systems*. Asilomar Conference on Signals, Systems and Computers, pp. 1-5, 2013.

42. N. Sandoval, C. Mackin, S. Whitsitt, R. Lysecky, J. Sprinkle. *System Throughput Optimization and Runtime Communication Middleware Supporting Dynamic Software-Hardware Task Migration in Data Adaptable Embedded Systems*. IEEE International Conference on Engineering of Computer-Based Systems (ECBS), pp. 59-68, 2013.

43. L. Ding, A. Lizarraga, S. Lysecky, R. Lysecky, A. Gordon-Ross. *Accuracy-Guided Runtime Adaptive Profiling Optimization of Wireless Sensor Networks*. IEEE International Conference on Engineering of Computer-Based Systems (ECBS), pp. 82-91, 2013.

44. J. C. Lee, R. Lysecky. *System Observation of Blocking, Non-Blocking, and Cascading Events for Runtime Monitoring of Real-Time Systems*. IEEE International Conference on Engineering of Computer-Based Systems (ECBS), pp. 49-58, 2013.

45. B. P. Zeigler, D. Kim, C. Seo, T. Pifer, R. Lysecky. *Linking Activity to Information and Energy in Hardware*, Activity-Based Modeling & Simulation (ACTIMS) 2012, ITM Web of Conferences, pp. 1-10, 2013.

46. J. C. Lee, F. Kouteib, R. Lysecky. *Event-Driven Framework for Configurable Runtime System Observability for SOC Designs*. International Test Conference (ITC), pp. 1-10, 2012.

47. S. Whitsitt, J. Sprinkle, R. Lysecky. *An Overseer Control Methodology for Data Adaptable Embedded Systems*. International Workshop on Multi-Paradigm Modeling (MPM), pp. 1-6, 2012.

48. J. Mu, R. Lysecky. *Adaptive Online Heuristic Performance Estimation and Power Optimization for Reconfigurable Embedded Systems*. International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS), pp. 265-274, 2012.

49. V. K. Nileshwar, R. Lysecky. SNR Analysis *Approach for Hardware/Software Partitioning using Dynamically Adaptable Fixed Point Representation*. ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 27-32, 2012.

50. A. Milakovich, V. S. Gopinath, R. Lysecky, J. Sprinkle. *Automated Software Generation and Hardware Coprocessor Synthesis for Data-Adaptable Reconfigurable Systems*. IEEE International Conference on Engineering of Computer-Based Systems (ECBS), pp. 15-23, 2012.

51. A. Munir, A. Gordon-Ross, S. Lysecky, R. Lysecky. *Online Algorithms for Wireless Sensor Networks Dynamic Optimization*. IEEE Consumer Communications and Networking Conference (CCNC), pp. 180-187, 2012.

52. V. S. Gopinath, J. Sprinkle, R. Lysecky. *Modeling of Data Adaptable Reconfigurable Embedded Systems*. IEEE Workshop on Model-Based Development for Computer Based Systems, pp. 276-283, 2011.

53. J. C. Lee, A. S. Gardner, R. Lysecky. *Hardware Observability Framework for Minimally Intrusive Online Monitoring of Embedded Systems*. IEEE International Conference on Engineering of Computer-Based Systems (ECBS), pp. 52-60, 2011.

54. S. Mahadevan, V. S. Gopinath, R. Lysecky, J. Sprinkle, J. Rozenblit, M. W. Marcellin. *Hardware/Software Communication Middleware for Data Adaptable Embedded Systems*. IEEE International Conference on Engineering of Computer-Based Systems (ECBS), pp. 34-43, 2011. **Received Best Paper Award**

55. A. Milakovich, V. Gopinath, R. Lysecky, J. Sprinkle. *Automated Software Generation and Hardware Coprocessor Synthesis for Data-Adaptable Reconfigurable Systems*. Workshop on Adaptive and Reconfigurable Embedded Systems (APRES), 2011.

56. Mu, J., R. Lysecky. *Profile Assisted Online System-Level Performance and Power Estimation for Dynamic Reconfigurable Embedded Systems*. Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 737-742, 2011.

57. J. Sun, R. Zheng, J. Velamala, Y. Cao, R. Lysecky, K. Shankar, J. Roveda. *A Self-Evolving Design Methodology for Power Efficient Multi-core Systems*. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 264-268, 2010.

58. A. Munir, A. Gordon-Ross, S. Lysecky, R. Lysecky. *A One-Shot Dynamic Optimization Methodology for Wireless Sensor Networks*. International Conference on Mobile Ubiquitous Computing, Systems, Services (UBICOMM), 2010. **Received Best Paper Award**

59. A. Munir, A. Gordon-Ross, S. Lysecky, R. Lysecky. *A Lightweight Dynamic Optimization Methodology for Wireless Sensor Networks*. IEEE International Conference on Wireless and Mobile Computing, Networking and Communications (WiMob), pp. 129-136, 2010.

60. J. Hiner, A. Shenoy, R. Lysecky, S. Lysecky, A. Gordon-Ross. *Transaction-Level Modeling for Sensor Networks Using SystemC*. IEEE International Conference on Sensor Networks, Ubiquitous, and Trustworthy Computing (SUTC), pp. 197-204, 2010.

61. J. Sun, R. Lysecky, K. Shankar, A. Kodi, A. Louri, J. Wang. *Workload Capacity Considering NBTI Degradation in Multi-core Systems*. Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 450-455, 2010.

62. K. Shankar, R. Lysecky. *Non-Intrusive Dynamic Application Profiling for Multitasked Applications*. Design Automation Conference (DAC), pp. 130-135, 2009.

63. L. Saldanha, R. Lysecky. *Hardware/Software Partitioning of Floating Point Software Applications to Fixed-Pointed Coprocessor Circuits*. IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS), pp. 49-54, 2008. **Received Best Paper Award**

64. A. Nair, R. Lysecky. *Non-Intrusive Dynamic Application Profiler for Detailed Loop Execution Characterization*. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), pp. 23-30, 2008.

65. M. Hammerquist, R. Lysecky. *Design Space Exploration for Application-Specific FPGAs in System-on-a-Chip Designs*. IEEE System on a Chip Conference (SOCC), pp. 279-282, 2008.

66. R. Lysecky. *Low-Power Warp Processor for Power Efficient High-Performance Embedded Systems*. IEEE/ACM Design Automation and Test in Europe Conference (DATE), pp. 141-146, 2007.

67. D. Sheldon, R. Kumar, R. Lysecky, F. Vahid, D. M. Tullsen. *Application-Specific Customization of Parameterized FPGA Soft-Core Processors*. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 261-268, 2006.

68. D. Sheldon, R. Kumar, F. Vahid, D. M. Tullsen, R. Lysecky. *Conjoining Soft-Core FPGA Processors*. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 694-701, 2006.

69. R. Lysecky, F. Vahid, S. Tan. *A Study of the Scalability of On-Chip Routing for Just-in-Time FPGA Compilation*. IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), pp. 57-62, 2005.

70. R. Lysecky, F. Vahid. *A Study of the Speedups and Competitiveness of FPGA Soft Processor Cores using Dynamic Hardware/Software Partitioning*. IEEE/ACM Design Automation and Test in Europe Conference (DATE), pp. 18-23, 2005.

71. R. Lysecky, K. Miller, F. Vahid, K. Vissers. *POSTER: Firm-core Virtual FPGA for Just-in-Time FPGA Compilation*. ACM International Symposium on Field-Programmable Gate Arrays (FPGA), pp. 271-271, 2005.

72. R. Lysecky, F. Vahid, S. Tan. *Dynamic FPGA Routing for Just-in-Time FPGA Compilation*. IEEE/ACM Design Automation Conference (DAC), pp. 954-959, 2004.

73. R. Lysecky, F. Vahid. *A Configurable Logic Architecture for Dynamic Hardware/Software Partitioning*. IEEE/ACM Design Automation and Test in Europe Conference (DATE), pp. 480-485, 2004.

74. C. Zhang, F. Vahid, R. Lysecky. A Self-Tuning Cache Architecture for Embedded Systems. IEEE/ACM Design Automation and Test in Europe Conference (DATE), pp. 16-20, 2004.

75. R. Lysecky, F. Vahid. *A Codesigned On-chip Logic Minimizer*. IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 109-113, 2003.
76. R. Lysecky, F. Vahid. *On-chip Logic Minimization*. IEEE/ACM Design Automation Conference (DAC), pp. 334-337, 2003.
77. G. Stitt, R. Lysecky, F. Vahid. *Dynamic Hardware/Software Partitioning: A First Approach*. IEEE/ACM Design Automation Conference (DAC), pp. 250-255, 2003.
78. R. Lysecky, S. Cotterell (Lysecky), F. Vahid. *A Fast On-Chip Profiler Memory*. IEEE/ACM Design Automation Conference (DAC), pp. 28-33, 2002.
79. G. Stitt, F. Vahid, T. Givargis, R. Lysecky. *A First-step towards an Architecture Tuning Methodology for Low Power*. IEEE/ACM International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), pp. 187-192, 2000.
80. R. Lysecky, F. Vahid, and T. Givargis. *Experiments with the Peripheral Virtual Component Interface*. IEEE/ACM International Symposium on System Synthesis (ISSS), pp. 221-224, 2000.
81. R. Lysecky, F. Vahid, and T. Givargis. *Techniques for Reducing Read Latency in Core Bus Wrappers*. IEEE/ACM Design Automation and Test in Europe Conference (DATE), pp. 84-91, 2000. **Received Best Paper Award**
82. R. Lysecky, F. Vahid, T. Givargis, and R. Patel. *Pre-fetching for Improved Core Interfacing*. IEEE/ACM International Symposium on System Synthesis (ISSS), pp. 51-55, 1999.

Technical Reports

1. Hammerquist, M. R. Lysecky. *A Technical Report on Design Space Exploration and CLB Customization for Application-Specific FPGAs*. University of Arizona Technical Report UA-041010-RL-02, pp. 1-9, 2010.
2. Shankar, K., R. Lysecky. *A Technical Report on Non-Intrusive Dynamic Application Soft Error Detection*. University of Arizona Technical Report UA-031510-RL-01, pp. 1-7, 2010.
3. J. Villarreal, R. Lysecky, S. Cotterell (Lysecky), F. Vahid. *Loop Analysis of Embedded Applications*. UC Riverside Technical Report UCR-CSE-01-03, 2001.

EQUIPMENT & SOFTWARE DONATIONS

1. Xilinx, Inc., Donation of Xilinx Vivado System Edition, Commercial Value: $1099, 2016.
2. Intel, Corp., Donation of DE 2i-150 Embedded Development Boards, $1500, 2013.
3. Xilinx, Inc., Donation of Virtex-6 (ML605) FPGA development board, Commercial Value: $1795, 2012.
4. Xilinx, Inc., Donation of Xilinx ISE and Vivado HLS Tool Suite, Commercial Value: $495, 2012.
5. Xilinx, Inc., Donation of Xilinx ISE and AutoESL Tool Suites, Commercial Value: $20,999, 2011.
6. Microchip, Inc. Donation of 12 PICKit 3 In-Circuit Debuggers and two 16-bit 28-pin Starter Boards, Commercial Value: $700, 2010.
7. Xilinx, Inc., Donation of Virtex5-FX (ML507) FPGA development board and 25-seat license for Xilinx ISE Design Suite 11, Commercial Value: $26,170, 2010.
8. Xilinx, Inc., Donation of Xilinx ISE, EDK, ChipScope Pro, and System Generator for DSP Tool Suites, Commercial Value: $22,300, 2006 – 2010.
9. Xilinx, Inc., Donation of 10 Spartan-3E FPGA development boards, Commercial Value: $1490, 2006.

10. Intel Corp., Donation of quad-core Intel Xeon server and two dual-core Pentium workstations, Commercial Value: $6800, 2006.
11. Xilinx Inc., Donation of two Virtex-4 FX (ML403) FPGA development boards, Commercial Value: $1200, 2005.
12. Xilinx, Inc., Donation of Spartan-3 and Virtex-II Pro (ML310) FPGA development boards and Xilinx ISE, EDK, ChipScope Pro, and System Generator for DSP Tool Suites, Commercial Value: $7500, 2005.

INVITED TALKS, TUTORIALS, PANELS, AND PRESENTATIONS

1. *Online Materials and Teaching for CS/CE: Research, Experiences, and Recommendations for Going Online due to COVID-19*. Annual ACM Southeast Conference, Tampa, FL, April 2020. (Keynote)
2. *Improving CS/CE Education: Recent Research and Experiences*. Consortium for Computing Sciences in Colleges: Midwest, Lisle, IL, October 2019. (Keynote)
3. *Challenges in Healthcare Simulation—Clinical and Research Perspectives*. Modeling and Simulation in Medicine, Spring Simulation Conference, Tucson, AZ, May 2019. (Panel)
4. *Reducing the Impact of Medical Device Hacks on Patients.* Health Journalism 2018, Phoenix, AZ, April 2018. (Invited Talk & Panel)
5. *Becoming Hackproof in Medtech Through Engineering.* The MedTech Forum 2018, Brussels, Belgium, January 2018. (Invited Talk & Panel)
6. *The Internet of Good Things and Bad Things*, University of Arizona, Aerospace and Mechanical Engineering Seminar, Tucson, AZ, November 2017.
7. *Runtime Anomaly Detection (RAD)*, Colorado State University, Fort Collins, CO, February 2017. (Invited Talk)
8. *Runtime Anomaly Detection (RAD)*, University of California, Irvine, November 2016. (Invited Talk)
9. *The SOC Whisperer*, University of Illinois, Chicago, April 2015. (Invited Talk)
10. *Stop Teaching with One Hand Tied Behind Your Back*, ACM Technical Symposium on Computer Science Education (SIGCSE), March 2015.
11. *The Real Power of the Web for Computing/Engineering Education*, University of Missouri - Kansas City, March 2015. (Invited Talk)
12. *The SOC Whisperer*, Northeastern University, Boston, MA, October 2014. (Invited Talk)
13. *Dynamically Adaptable Embedded Systems*, Eta Kappa Nu, April 2014. (Invited Talk)
14. *Data-driven Design Methods and Optimization for Adaptable High-Performance Systems*, Oak Ridge National Laboratory, January 2014. (Invited Talk)
15. *Efficient Reconfiguration Methods to Enable Rapid Deployment of Runtime Reconfigurable Systems*, 47th Asilomar Conference on Signals, Systems and Computers (Invited Talk), Pacific Grove, CA, 2013.
16. *How You Can Learn to Stop Worrying and Love Reconfigurable Embedded Systems: A Tutorial*. IEEE International Conference and Workshops on the Engineering of Computer Based Systems (ECBS), Phoenix, AZ, 2013.
17. *Modeling and Codesign Methods for Data Adaptable Reconfigurable Embedded Systems*, University of Arkansas, October 2011. (Invited Talk)
18. *Data Adaptability, Dynamic Reconfiguration, and Online Monitoring/Optimization for Embedded Systems*, Raytheon Industry Day, University of Arizona, October 2011.

19. *Hardware Observability Framework for Non-Intrusive Monitoring of Complex Embedded Systems*, Workshop on Compiler Assisted System-on-Chip Assembly (CASA), October 2010. (Invited Talk)
20. *Dynamic and Autonomous Software-to-Hardware Translation for High-Performance and Low-Power Embedded Computing*, ECE Currents, University of Arizona, Tucson, AZ, August 2009.
21. *Dynamic and Autonomous Software-to-Hardware Translation for High-Performance and Low-Power Embedded Computing*, Computer Engineering and Computer Science Seminar, University of Arizona, Tucson, AZ, March 2009 (Invited Talk).
22. *Autonomously Adaptive Computing: Coping with Scalability, Reliability, and Dynamicity in Future Generations of Computing*, Kavli/NNIN Symposium on Computing, Cornell University, Ithaca, NY, October 2008 (Invited Talk).
23. *Warp Processing for Reliability and Prognostics*, Ridgetop Group, Tucson, AZ, September 2006. (Invited Talk)
24. *Warp Processors*, Honeywell, Tucson, AZ, August 2006. (Invited Talk)
25. *Warp Processors*, Intel Research, Intel Corp., Santa Clara, CA, June 2006. (Invited Talk)
26. *Low Power FPGAs*, ECE Currents, University of Arizona, Tucson, AZ, April 2006.
27. *Operating System Aware HW/SW Partitioning*, ECE Currents, University of Arizona, Tucson, AZ, October 2005.
28. *Warp Processors*, Tucson Embedded Systems (presented at University of Arizona), Tucson, AZ, August 2005.
29. *Warp Processors*, Intel Research, Intel Corp., Santa Clara, CA, February 2005. (Invited Talk)
30. *Warp Processors*, Xilinx, Inc. (presented at University of California, Riverside), Riverside, CA, 2004.
31. *Warp Processors*, Philips Electronics (presented at University of California, Riverside), Riverside, CA, 2004.
32. *On-Chip Logic Minimization for IP Routing Table and ACL Reduction*, Procket Networks, Inc. (presented at University of California, Riverside), Riverside, CA, 2002. (Invited Talk)
33. *Pre-fetching for Improved Core Interfacing*, VLSI Technologies, Illinois, 2000. (Invited Talk)

MEDIA

1. *UA engineers collaborate on $3.5M DOE traffic-flow project*. EurekaAlert!, March 12, 2020.
2. *Tech Blog: Automated Malware Detection for Life-Critical Systems*, A. Mairena, Tech Launch Arizona, May 28, 2019.
3. *Road test shows some adaptive cruise control systems can amplify phantom jams*, Vanderbilt University, EurekaAlert!, May 08, 2019.
4. *Medical device security: Hacking prevention measures,* Y. Grauer, Hewlett Packard Enterprise.nxt, June 25, 2018.
5. *The Lurking Danger of Medical Device Hackers*, Y. Grauer, Donald W. Reynolds National Center for Business Journalism, May 23, 2018.
6. *What to ask hospitals about medical device hacking preparedness*, R. Vesely, Association of Health Care Journalists, Apr 25, 2018.
7. *Medicine pumps & Pacemaker threat as Dr's simulate hacked overdose*, W. Amir, HackRead, Apr 20, 2018.
8. *Hackers pose danger to patients with pacemakers, other medical devices connected to internet*, F. Miller, Cronkite News, Apr 19, 2018.

9. *Keeping medical devices safe from cybersecurity threats*, K. Lant., Samsung Next, Feb 08, 2018.
10. *To beat the hackers, we need to design secure medical devices*, MedTech Views, Jan 18, 2018.
11. *Cardi-Hack*, National Science Foundation, "The Discovery Files", May 31, 2017.
12. *Under attack: How safe is your connected medical device*? Medical Plastics News, May 09, 2017.
13. *UA researchers working to stay a step ahead of medical device hackers*, Tucson News Now (aired on KOLD, Tucson AZ), March 22, 2017.
14. *Protecting implanted medical devices (IMDs) from side-channel attacks*, Rambus, March 21, 2017.
15. *How a UA Engineer Stays a Heartbeat Ahead of Hackers*, UA News, March 15, 2017.
16. *Protecting Implantable Medical Devices from Malware, Side-Channel Attacks*, Med Device Online, March 10, 2017.
17. *Reimagined Textbooks Adapt to Student Learning,* UA News, October 14, 2015.
18. *Changing How Students Learn*, UCR Today, April 13, 2015.
19. *Goal of researcher at UA: Let you gab longer on cell*, Arizona Daily Star, April 15, 2009.
20. *Warp Power May Soon Add Extra Life to Your Cell Phone and iPod Batteries*, UA News, April 14, 2009.
21. *Whitepaper: Navigating the Research Funding Environment*, Elsevier Research Intelligence, May 2009.

PROFESSIONAL ACTIVITIES

Co-Director

- Co-Director, Arizona Center for Integrative Modeling and Simulation (ACIMS), 2010 – Present.

Editorial & Conference Organization

- Associate Editor, IEEE Transactions of Computers, 2019 – Present.
- Program Committee Chair, International Conference on Hardware - Software Codesign and System Synthesis (CODES+ISSS), 2020.
- Program Committee Vice Chair, International Conference on Hardware - Software Codesign and System Synthesis (CODES+ISSS), 2019.
- Publications Chair, Embedded Systems Week (ESWEEK): International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), International Conference on Hardware - Software Codesign and System Synthesis (CODES+ISSS), and International Conference on Embedded Software (EMSOFT), 2018.
- Discussion Manager, IEEE/ACM Conference on Hardware Software Codesign and System Synthesis (CODES+ISSS), 2018.
- Track Co-Chair, IEEE/ACM Conference on Hardware Software Codesign and System Synthesis (CODES+ISSS), 2017.
- Publicity Chair, North America, Embedded Systems Week (ESWEEK), 2014.
- Program Co-Chair, Modeling and Simulation in Medicine, Summer Simulation Multi-Conference, 2014.
- Publications Chair, Embedded Systems Week (ESWEEK): International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), International Conference on Hardware -

Software Codesign and System Synthesis (CODES+ISSS), and International Conference on Embedded Software (EMSOFT), 2010 – 2011.

- Editorial Board, IET Computers & Digital Techniques, 2009 – 2012.
- Associate Editor, Simulation: Transactions of the Society for Modeling and Simulation International, 2006 – 2008.
- Web Chair, 13th International Symposium on High-Performance Computer Architecture (HPCA), 2006 – 2007.

Technical Program Committee

- IEEE/ACM Conference on Hardware Software Codesign and System Synthesis (CODES+ISSS), 2010 – 2021.
- Languages, Compilers, Tools and Theory of Embedded Systems (LCTES), 2019.
- ACM Technical Symposium on Computer Science Education (SIGCSE), 2017 – 2018.
- IEEE/ACM Design and Test in Europe Conference (DATE), 2007 – 2011, 2015 – 2017.
- IEEE/ACM Design Automation Conference (DAC), 2013 – 2015.
- IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), 2010 – 2015.
- IEEE Conference on Embedded and Ubiquitous Computing (EUC), 2014 – 2015.
- ACM SIGDA Ph.D. Forum at the Design Automation Conference (DAC), 2007 – 2015.
- IEEE Conference on Field Programmable Logic and Applications (FPL), 2007 – 2015.
- International Conference on ReConFigurable Computing and FPGAs (ReConFig), 2013 – 2015.
- IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2013.
- IEEE International Conference on the Engineering of Computer Based Systems (ECBS), 2007 – 2013.
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2012.
- IEEE/ACM Design and Test in Europe Conference (DATE), 2007 – 2011.
- IEEE Eastern European Conference on the Engineering of Computer Based Systems (ECBS-EERC), 2008 – 2011.
- IEEE International Symposium on Quality Electronic Design (ISQED), 2007 – 2009.
- International Conference on Embedded Software and Systems (ICESS), 2007.

Session Chair/Co-Chair

- Session Chair, Medical Simulation, Modeling and Simulation in Medicine, Spring Simulation Conference, Tucson, AZ, April 2019.
- Session Chair, Power Efficient Deigns, IEEE/ACM International Conference on Hardware/Software Codesign and Systems Synthesis (CODES+ISSS), Torino, Italy, October 2018.
- Session Chair, Reliability and Robustness, IEEE/ACM International Conference on Hardware/Software Codesign and Systems Synthesis (CODES+ISSS), Pittsburgh, PA, October 2016.
- Special Session Organizer and Chair, Runtime Adaptive Embedded Systems and Architectures, International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), July 2011.

- Session Co-Chair, Session 4A, MPSoC: Analysis and Synthesis, IEEE/ACM International Conference on Hardware/Software Codesign and Systems Synthesis (CODES+ISSS), Scottsdale, AZ, October 2010.
- Session Chair, Session 8B, System Level Power Modeling and Optimization, IEEE/ACM International Conference on Hardware/Software Codesign and Systems Synthesis (CODES+ISSS), Atlanta, GA, October 2008.
- Session Chair, Session 42.1, Multi-core Design Tools and Architectures, IEEE/ACM Design Automation Conference (DAC), Anaheim, CA, 2008.
- Session Chair, Session 2.7, Design Space Exploration and Nano-Technologies for Reconfigurable Computing, IEEE/ACM Design and Test in Europe Conference (DATE), Nice, France, April 2007.

Reviewer

- IEEE Security & Privacy (S&P)
- IEEE Transactions on Dependable and Secure Computing (TDSC)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computer Aided Design (TCAD)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Design & Test
- IEEE Embedded Systems Letters (ESL)
- IEEE Communication Letters (CL)
- IEEE Transactions on Signal Processing (TSP)
- IEEE Transactions on Parallel and Distributed Systems (TPDS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Transactions on Embedded Computing Systems (TECS)
- ACM Transactions on Reconfigurable Technology and Systems (TRTS)
- ACM Transactions on Architectures and Code Optimization (TACO)
- ASEE Advances in Engineering Education (AEE)
- IET Computers and Digital Techniques (IET-CDT)
- Journal on Design Automation of Embedded Systems (DAEM)
- International Journal of Parallel Programming (IJPP)
- International Journal of High Performance Systems Architecture (IJHPSA)
- Microelectronics Journal (MEJ)
- Journal of Systems Architecture (JSA)
- Journal of Systems and Software (JSS)
- International Journal of Computers and Electrical Engineering (IJCEE)
- International Journal of Reconfigurable Computing (IJRC)
- Journal of Aerospace Computing, Information, and Communication (JACIC)
- Journal of Future Generation Computer Systems (FGCS)

University, College, and Department Committees

- University of Arizona, General Petitions Committee, Chair, 2021 – Present.
- College of Engineering, College Advisory Committee, 2011, 2018 – Present.
- ECE, Committee on Committees, 2012 – Present.
- ECE, Undergraduate Studies Committee, 2012 – 2016, 2017 – 2020.
- University of Arizona, General Petitions Committee, Co-chair, 2018 – 2020.
- University of Arizona, General Petitions Committee, 2017 – 2018.
- University of Arizona, Undergraduate STEM Education Leadership Committee, 2014 – 2018.
- University of Arizona, Faculty Senate, 2012 – 2014.
- ECE, Executive Committee, 2013 – 2014.
- ECE, Computer Policy Committee, 2006 – 2008, 2011 – 2012, 2014 – 2015
- ECE, Peer Review Committee, 2012 – 2013.
- ECE, Graduate Recruiting and Awards Committee, 2010 – 2012.
- College of Engineering, Outstanding Teaching Assistant Awards Committee, 2012.
- ECE, Peer Review Committee, 2009 – 2010.
- ECE, Undergraduate Studies Committee, 2008 – 2009.
- ECE, Undergraduate Recruiting and Awards Committee, 2008 – 2009.

PROFESSIONAL MEMBERSHIPS

- Institute of Electrical and Electronics Engineers (IEEE), Senior Member
- Association for Computing Machinery (ACM), Senior Member
- American Society of Engineering Education (ASEE)
- IEEE Computer Society (CS)
- ACM Special Interest Group on Design Automation (SIGDA)
- ACM Special Interest Group on Computer Science Education (SIGCSE)

COURSES TAUGHT

- ECE 413/513 – Web Programming and the Internet of Things, Fall 2020.
- ECE 413/513 – Web Programming and the Internet of Things, Fall 2019.
- ECE 413/513 – Web Programming and the Internet of Things, Fall 2018.
- ECE 413/513 – Web Programming and the Internet of Things, Fall 2017.
- ECE 275 – Computer Programming II, University of Arizona, Spring 2016.
- ECE 576B – Embedded Systems Design and Optimization, University of Arizona, Spring 2016.
- ECE 474a/574a – Computer-Aided Logic Design, University of Arizona, Fall 2015.
- ECE 474a/574a – Computer-Aided Logic Design, University of Arizona, Fall 2014.

- ECE 275 – Computer Programming II, University of Arizona, Fall 2013.
- ECE 576 – Engineering of Computer Based Systems, University of Arizona, Spring 2013.
- ECE 274 – Digital Logic, University of Arizona, Fall 2012.
- ECE 275 – Computer Programming II, University of Arizona, Fall 2012.
- ECE 576 – Engineering of Computer Based Systems, University of Arizona, Spring 2012.
- ECE 275 – Computer Programming II, University of Arizona, Fall 2011.
- ECE 576 – Engineering of Computer Based Systems, University of Arizona, Spring 2011.
- ECE 372 – Microcontroller Design, University of Arizona, Fall 2010.
- ECE 474a/574a – Computer-Aided Logic Design, University of Arizona, Fall 2010.
- ECE 474a/574a – Computer-Aided Logic Design, University of Arizona, Spring 2010.
- ECE 576 – Engineering of Computer Based Systems, University of Arizona, Spring 2010.
- ECE 274 – Digital Logic, University of Arizona, Fall 2009.
- ECE 576 – Engineering of Computer Based Systems, University of Arizona, Spring 2009.
- ECE 274 – Digital Logic, University of Arizona, Spring 2009.
- ECE 274 – Digital Logic, University of Arizona, Fall 2008.
- ECE 576 – Engineering of Computer Based Systems, University of Arizona, Spring 2008.
- ECE 274 – Digital Logic, University of Arizona, Spring 2008.
- ECE 274 – Digital Logic, University of Arizona, Fall 2007.
- ECE 576 – Engineering of Computer Based Systems, University of Arizona, Spring 2007.
- ECE 372 – Microcontroller Design, University of Arizona, Fall 2006.
- ECE 576 – Engineering of Computer Based Systems, University of Arizona, Spring 2006.
- ECE 274 – Digital Logic, University of Arizona, Fall 2005.
- CS 168 – VLSI Design, University of California, Riverside, Winter 2004.

GRADUATE STUDENTS

PhD

- Aakarsh Rao, ECE PhD Candidate
- Nadir Carreon, ECE PhD Candidate
- Negar Zarei, ECE PhD Candidate
- Manoj Gopale, ECE PhD Student
- Yuchao Liao, ECE PhD Student
- Sofia Carreon, ECE PhD Student
- Bozhi Liu, ECE PhD, August 2020 (Lunewave)
- Minjun Seo, PhD ECE May 2018 (University of California, Irvine)
- Sixing Lu, PhD ECE, July 2017 (Microsoft, Redmond, WA)
- Hyunsuk Nam, PhD ECE, March 2017 (M2APPL, Inc., Seoul, Korea)

- Adrian Lizarraga, PhD ECE, May 2016 (zyBooks, Los Gatos, CA)
- Jong Chul Lee, PhD ECE, 2014 (eWBM, Seoul, Korea)
- Jingqing Mu, PhD ECE, 2011 (Oak Ridge National Laboratory, Oak Ridge, TN)

MS

- Jaewan Kim, ECE MS Student
- Sudarshan Sargur, MS ECE, December 2015 (Cisco, San Jose, CA)
- Nathan Sandoval, MS ECE, 2013 (General Dynamics, Scottsdale, AZ)
- Tim Pifer, MS ECE, 2011 (Intel, Hillsboro, OR)
- Lu Ding, MS ECE, 2011 (Western Digital, Lake Forest, CA)
- Vijay Shankar Gopinath, MS ECE, 2011 (Microsoft, Redmond, WA)
- Sundararajan Srinivasan, MS ECE, 2011 (Microsoft, Redmond, WA)
- Sachidanand Mahadevan, MS ECE, 2010 (Intel, Folsom, CA)
- Varadaraj Kamath Nileshwar, MS ECE, 2010 (NVIDIA, Santa Clara, CA)
- Jeffrey Hiner, MS ECE, 2010 (Sandia National Laboratories, Albuquerque, NM)
- Ashish Shenoy, MS ECE, 2010 (Riverbed, San Francisco, CA)
- Karthik Shankar, MS ECE, 2010 (NVIDIA, Santa Clara, CA)
- Andrew Gardner, ME ECE, 2009 (Raytheon, Tucson, AZ)
- Lance Saldanha, MS ECE, 2008 (V-Soft Consulting/Moore Medical)
- Mark Hammerquist, MS ECE, 2008 (Texas Instruments, Tucson, AZ)
- Rahul Kalra, MS ECE, 2007 (Motorola, San Diego, CA)
- Ajay Nair, MS ECE, 2007 (Western Digital, Lake Forest, CA)

UNDERGRADUATE STUDENTS

- Undergraduate students actively involved in research projects: Mitchell Dzurick, Lena Voytek, Swati Chandra, Marianne Madias, Christa Marie Sonderer, Andres Barragan, Cody Thivener, Sima Jalaleddine, Alli Gilbreath, Swati Munjal, Jake Given, Dalton Hirst, Jay Jackman, Nick Wohlleb, Daniela Ibarra, Shivani Patel, Justin Loera, Horacio Valencia, Joey McClanahan, Jonathan Torres, Casey Mackin, Brian Smith, David Schwartz, Jovan Vance, Maryam Abdul-Wahid, Adrian Lizarraga, Andrew Milakovich, Ernesto Rascon, Faycel Kouteib, Jesse Gunsch, Kyle Merry, Nathan Sandoval, Oscar Galvan, Poe Park, Uchenna Okeke, Vineet Dixit

OTHER HOBBIES & INTERESTS

- Woodworking: Furniture design and building.
- Motorcycling. Currently riding a Ducati Streetfighter 848.
- Photography (Digital and Film). Mainly using Leica M6 TTL and Voigtländer Bessa R2m rangefinders cameras, black and white film, and developing film at home.

- Homebrewing beer. Received multiple Silver and Bronze Certificates in First Round of 2012 and 2013 National Homebrew Competitions.