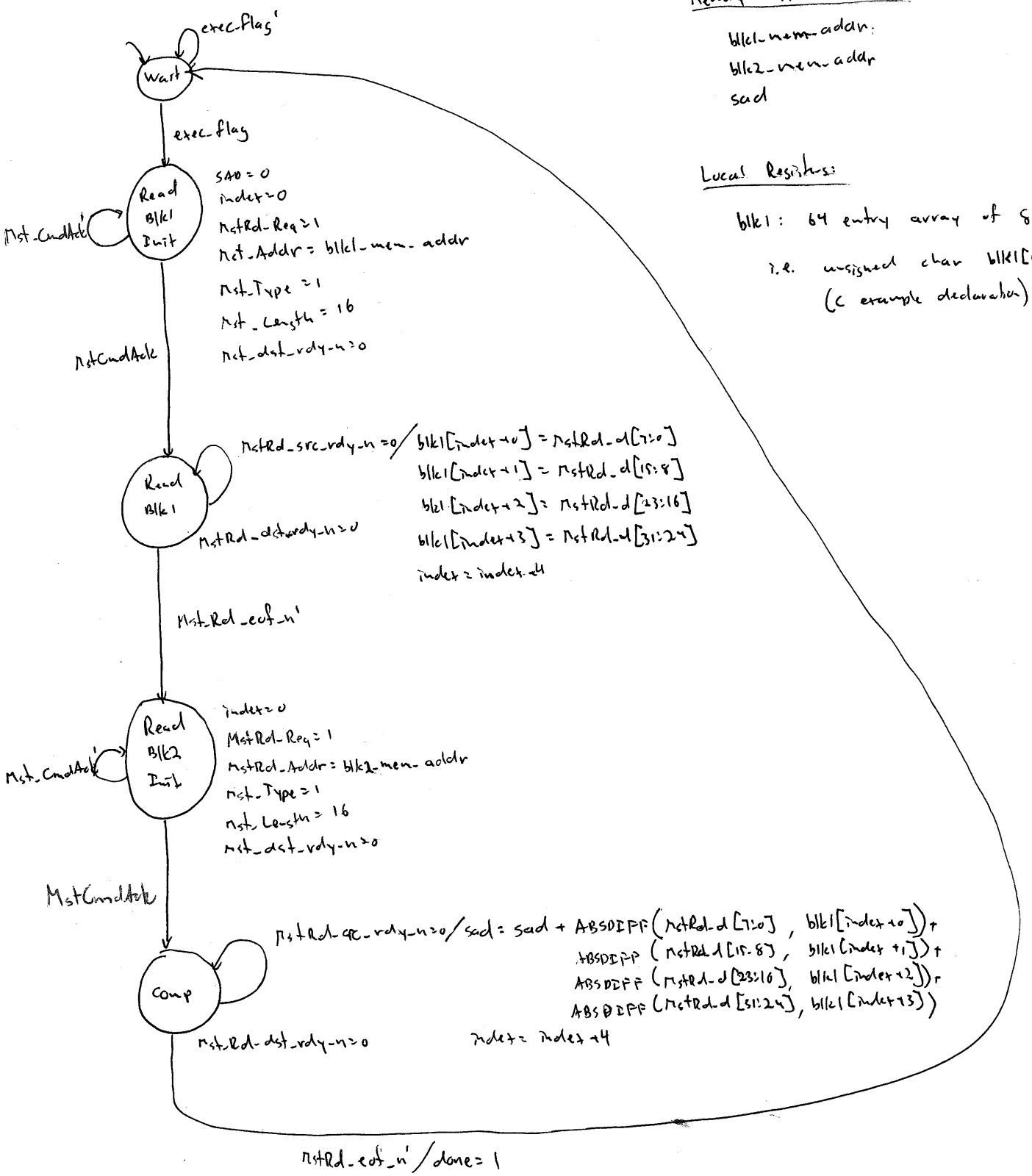
+ FSMD shown without error checking states/conditions for bus errors (i.e. this is an incompletely specified FSM)



Memory Mapped Registers:

- blk1_mem_addr
- blk2_mem_addr
- sad

Local Registers:

- blk1: 64 entry array of 8-bit values
  - i.e. unsigned char blk1[64]
    (C example declaration)

Performance Estimation (Best case): Simple

$$Time_{HW} = Execs * (2 + 64 + 2 + 64)$$

(64: ReadBlk1; 64: Comp; 2: Read Blk1 Init; 2: Read Blk2 Init)

$$= 328{,}014 * 132$$

$$= 43{,}297{,}848 \text{ cycles}$$

$$Time_{comm} = Execs * (3 + 3 + 3)$$

(3: blk2_mem_addr; 3: blk1_mem_addr; 3: send)

$$= 328{,}014 * 9$$

$$= 2{,}952{,}126 \text{ cycles}$$

$$Time_{sw\ (orig)} = 805{,}306{,}125 * 1.5 \text{ (CPI)} = 1{,}207{,}959{,}187 \text{ cycles}$$

$$Time_{hwsw} = (805{,}306{,}125 - 528{,}961{,}275) * 1.5 + 43{,}297{,}848 + 2{,}952{,}126$$

$$= 460{,}767{,}249 \text{ cycles}$$

$$S_{HWSW} = \underline{2.62X}$$

Performance Estimation (worst case): Simple

$Time_{HW}$ = Execs * (32 + 64 + 32 + 64)

cycles waiting for access to bus

= 328,014 * 192

= 62,978,688 cycles

$Time_{comm}$ = Execs * (33 + 33 + 33)

= 328,014 * 99

= 32,473,386 cycles

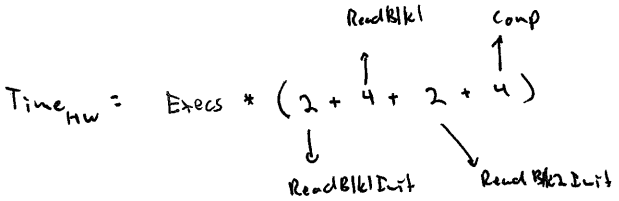
$Time_{HWSW}$ = (805,306,125 - 528,961,275) * 1.5 + 62,978,688 + 32,473,386

= 509,969,349 cycles

S_{HWSW} = 2.37X

Performance Estimation (Best case): Efficient

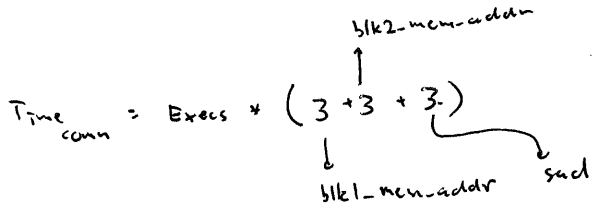
In the best case, the request for the blk1 and blk2 read take 2 cycles to receive the acknowledge and four cycles total for each blk data read.



$Time_{HW}$ = Execs * (2 + 4 + 2 + 4)

= 328014 * 5.54 * (12)

= 21,806,370 cycles



$Time_{comm}$ = Execs * (3 + 3 + 3)

= 328014 * 5.54 * (9)

= 16,354,779 cycles

$Time_{sw}$ = 805,306,125 * 1.5 = 1,207,959,187 cycles

(1.5 = CPI)

$Time_{hw/sw}$ = 805,306,125 * 1.5 - 528,961,275 * 1.5 + 21,806,370 + 16,354,779

= 414,517,275 + 21,806,370 + 16,354,779

= 452,678,424 cycles

$S = \frac{1,207,959,187}{452,678,424} = \underline{2.67X}$ (best case)

Software:

```
for (j=0; j<16; j++) {
    *blk1_mem_addr = blk1 + j*16;
    *blk2_mem_addr = blk2 + j*16;
    wait for Intr();
    s += *sad;
    if (s >= distlim) break;
}
```

Performance Estimation (worst case): Efficient

In the worst case (or near worst case) the bus request can take 32 cycles for the acknowledge:

$$Time_{HW} = Execs * (32 + 4 + 32 + 4)$$

$$= 324014 * 5.54\ (72)$$

$$= 130,838,224 \text{ cycles}$$

$$Time_{comm} = Execs * (33 + 33 + 33)$$

$$= 328014 * 5.54\ (99)$$

$$= 179,902,559 \text{ cycles}$$

$$Time_{HWSW} = 414,517,275 + 130,838,224 + 179,902,559$$

$$= 725,258,058 \text{ cycles}$$

$$S = \frac{1,207,454,187}{725,258,058} = \underline{1.67X} \text{ (worst case)}$$

Note: Communication dominates HW/SW execution, i.e. $Time_{comm} > Time_{HW}$

How can we further improve performance given bus latency?