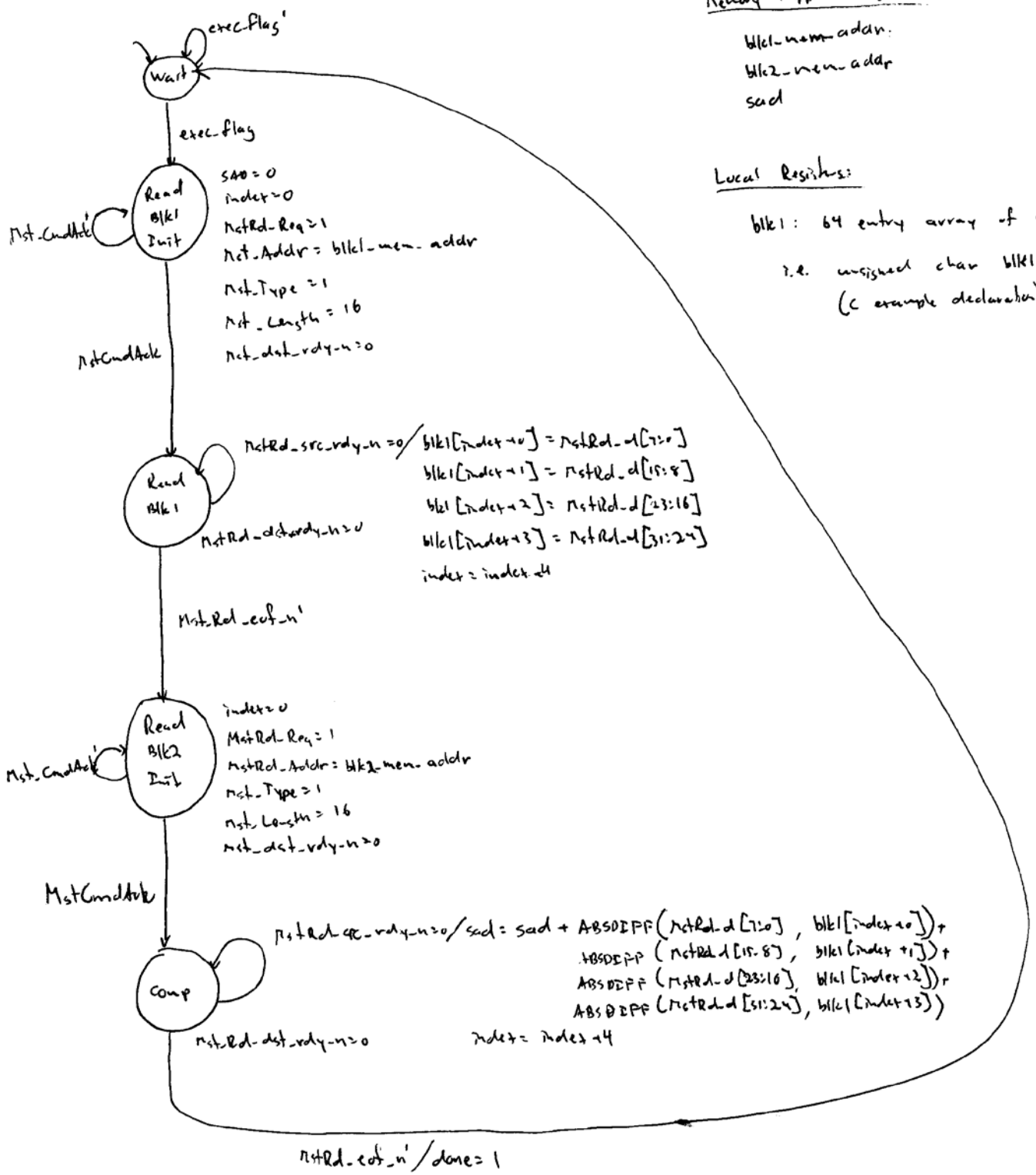
* FSMD shown without error checking states/conditions for bus errors (i.e. this is an incompletely specified FSM)



Memory Mapped Registers:

blk1_mem_addr
blk2_mem_addr
sad

Local Registers:

blk1: 64 entry array of 8-bit values

i.e. unsigned char blk1[64]
(C example declaration)

Performance Estimation (Best case):

In the best case, the request for the blk1 and blk2 read take 2 cycles to receive the acknowledge and four cycles total for each blk data read.

$$Time_{HW} = Execs * (\underbrace{2}_{\text{ReadBlk1Init}} + \overset{\text{ReadBlk1}}{4} + \underbrace{2}_{\text{ReadBlk2Init}} + \overset{\text{Comp}}{4})$$

$$= 328014 * 5.54 * (12)$$

$$= 21{,}806{,}370 \text{ cycles}$$

$$Time_{comm} = Execs * (\underbrace{3}_{\text{blk1\_mem\_addr}} + \overset{\text{blk2\_mem\_addr}}{3} + \underbrace{3}_{\text{sad}})$$

$$= 328014 * 5.54 * (9)$$

$$= 16{,}354{,}779 \text{ cycles}$$

Software:

```
for (j=0; j<16; j++) {
    *blk1_mem_addr = blk1 + j*16;
    *blk2_mem_addr = blk2 + j*16;
    wait for Intr();
    s += *sad;
    if (s >= distlim) break;
}
```

$$Time_{sw} = 805{,}306{,}125 * \underset{\text{CPI}}{1.5} = 1{,}207{,}959{,}187 \text{ cycles}$$

$$Time_{hw/sw} = 805{,}306{,}125 * 1.5 - 528941{,}275 * 1.5 + 21{,}806{,}370 + 16{,}354{,}779$$

$$= 414{,}517{,}275 + 21{,}806{,}370 + 16{,}354{,}779$$

$$= 452{,}678{,}424 \text{ cycles}$$

$$S = \frac{1{,}207{,}959{,}187}{452{,}678{,}424} = \underline{\underline{2.67\times}} \text{ (best case)}$$

Performance Estimation (worst case):

In the worst case (or near worst case) the bus request can take 32 cycles for the acknowledge:

$$Time_{HW} = Execs * (32 + 4 + 32 + 4)$$
$$= 328014 * 5.54\ (72)$$
$$= 130{,}838{,}224 \text{ cycles}$$

$$Time_{comm} = Execs * (33 + 33 + 33)$$
$$= 328014 * 5.54\ (99)$$
$$= 179{,}902{,}559 \text{ cycles}$$

$$Time_{HWSW} = 414{,}517{,}275 + 130{,}838{,}224 + 179{,}902{,}559$$
$$= 725{,}258{,}058 \text{ cycles}$$

$$S = \frac{1{,}207{,}454{,}187}{725{,}258{,}058} = \underline{\underline{1.67X}} \text{ (worst case)}$$

Note: Communication dominates HW/SW execution, i.e. $Time_{comm} > Time_{HW}$

How can we further improve performance given bus latency?