PRACTICE PROBLEM SET 4
Behavioral Synthesis

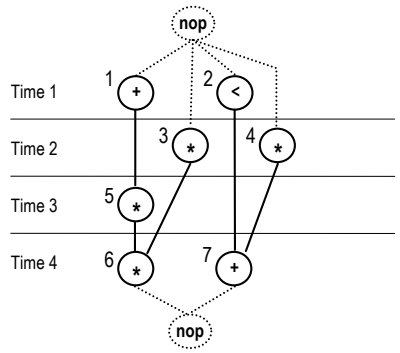
1. Identify which of the following algorithms is an unconstrained scheduling algorithm.
   (a) ASAP
   (b) ALAP
   (c) Hu
   (d) LIST_L
   (e) none of the above

2. Which of the following is a latency-constrained scheduling algorithm?
   (a) ASAP
   (b) Simulated Annealing
   (c) LIST_L
   (d) Graph Coloring
   (e) ALAP

3. Which of the following correspond to a phase of technology mapping?
   (a) Decomposition
   (b) Prime Implicant Generation
   (c) Covering
   (d) Reduce
   (e) Irredundant

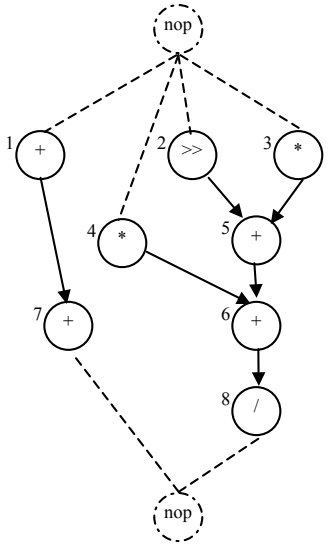
4. What is the mobility of node 7 in Figure 1?
   (a) 0
   (b) 1
   (c) 2
   (d) 3
   (e) 4

Fig 1: BDD used in Problem 4

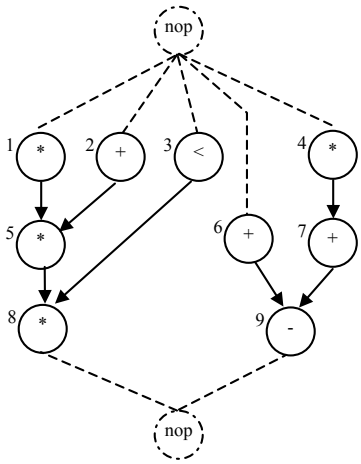


5. Which of the following provide canonical representations?
   (a) ROBDDs (reduced, ordered BDDs)
   (b) Sum-of-products
   (c) Truth table
   (d) Essential prime implicants
   (e) Sum-of-minterms

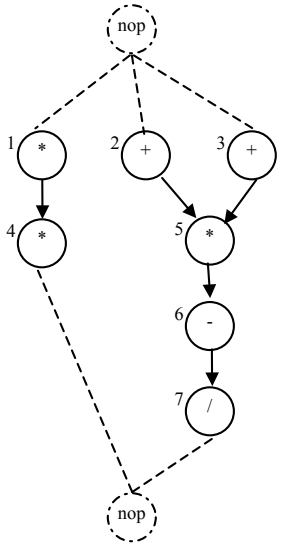
6. Determine the mobility of each node in the sequencing graph below.



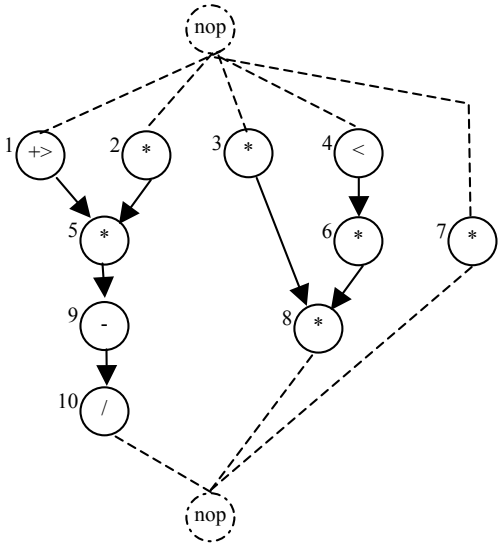
7. Utilizing Hu's algorithm, schedule the sequencing graph below assuming a = 2. Assume all operations require 1 cycle.



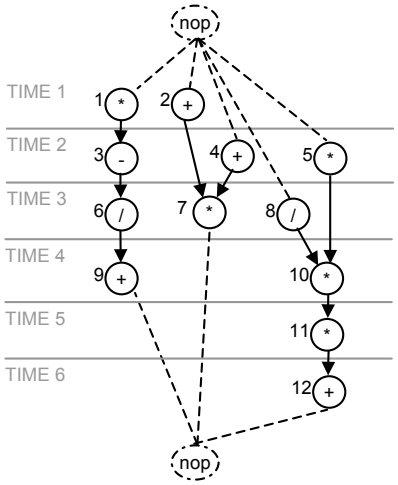
8. Utilizing the LIST_L algorithm, schedule the sequencing graph below assuming 2 multipliers and 1 ALU is available. Assume multiply operations require 2 cycles and ALU operations require 1 cycle.



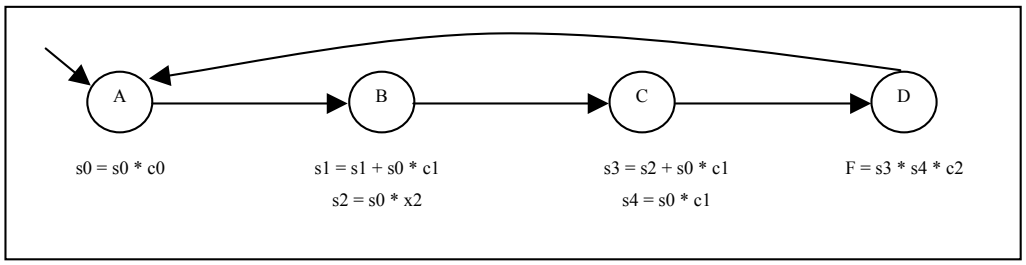
9. Utilizing the LIST_L algorithm, schedule the sequencing graph below assuming 2 multipliers and 1 ALU is available. Assume multiply operations require 2 cycles and ALU operations require 1 cycle. Show your work illustrating each iteration of the algorithm, as well as the final scheduled graph.



10. For the following sequencing graph
    (a) Create a compatibility graph for the following sequencing graph. Perform resource binding using the clique partitioning method.
    (b) Create a conflict graph, perform resource binding using the graph coloring method
    (c) Which method yields better results?



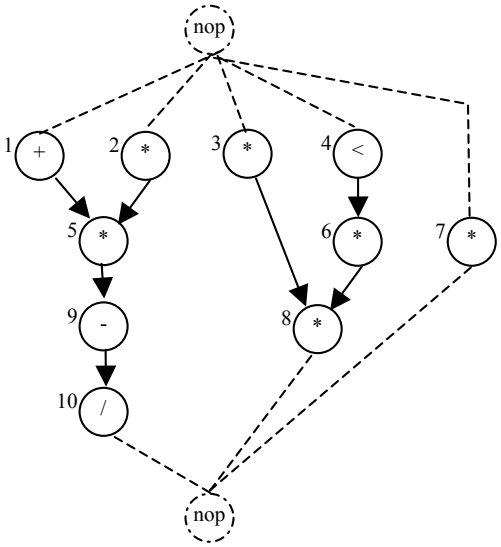
11. Given a high-level state machine below, create two different designs: one design optimized for minimum circuit speed and one design optimized for minimum circuit size. Be sure to clearly indicate the component allocation, operator binding, and operator scheduling used to design the two circuits.
    (a) Design optimized for minimum circuit speed.
    (b) Design optimized for minimum circuit size.



12. Given the sequencing graph in Fig. 3, utilize the LIST_R algorithm to determine the minimum number of multipliers and ALUs needed assuming

    (a) A latency constraint of 4
    (b) A latency constraint of 5

Fig 3. Gs(V,E) used in Problem 4.



13. (Force-Directed Scheduling) Assuming a latency of 4, find the following for the sequencing graph providing in Fig. 4

    (a) Time frame and width
    (b) Operation/Resource Probability
    (c) Forces for node 4
    (d) Forces for node 7

Fig 4. Gs(V,E) used in Problem 5.