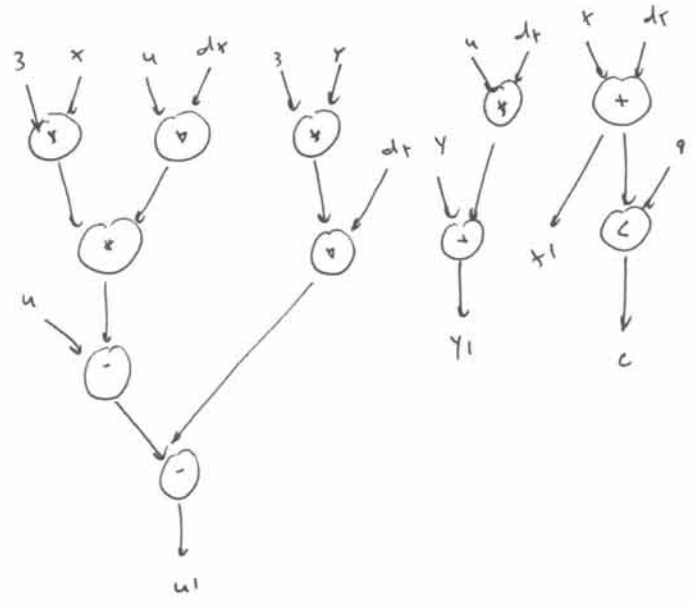
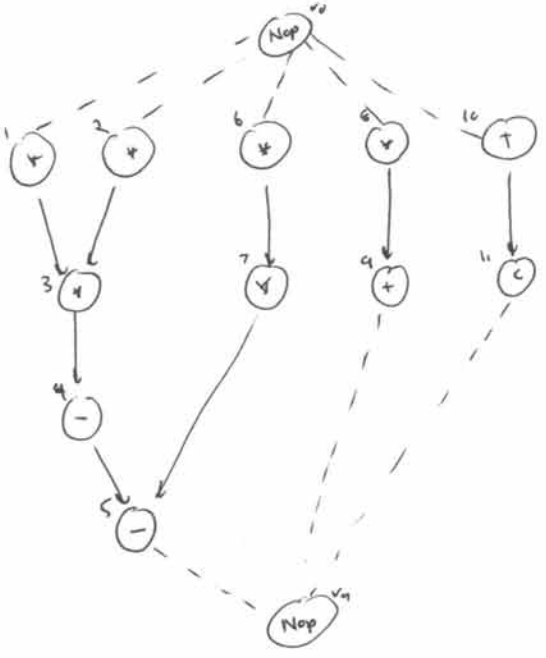
Sequential C Code:

```
x1 = x + dx
u1 = u - (3 * x * u * dx) - (3 * y * dx)
y1 = y + u * dx
c = x1 < a
```

CDFG (Control / Dataflow Graph):



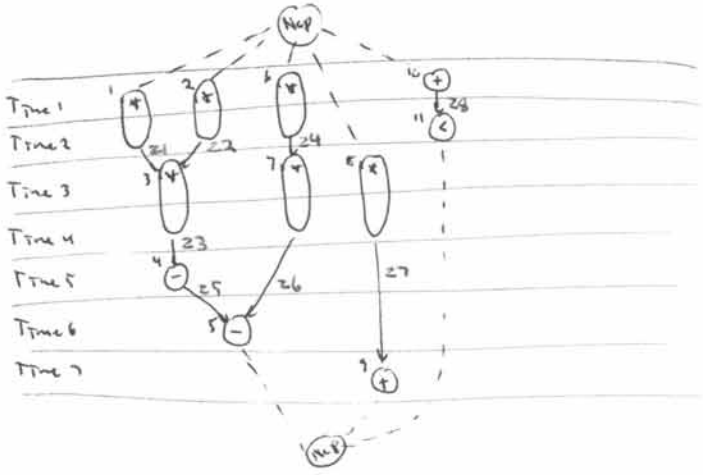
Sequencing Graph: (Unscheduled):



Scheduled Sequencing Graph:

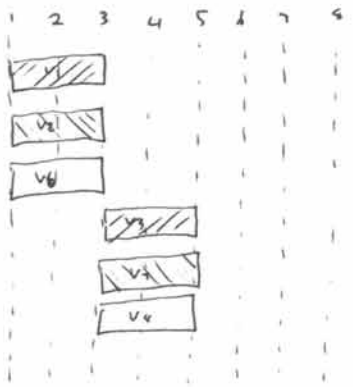
Mult = 2 cycles (3)
ALU = 1 cycle (1)

Resource constrained minimum latency (LIST_L)



Resource Sharing and Binding:

Multipliers:



LEFT-EDGE coloring:

MULT1: v_1, v_3

MULT2: v_2, v_7

MULT3: v_6, v_8

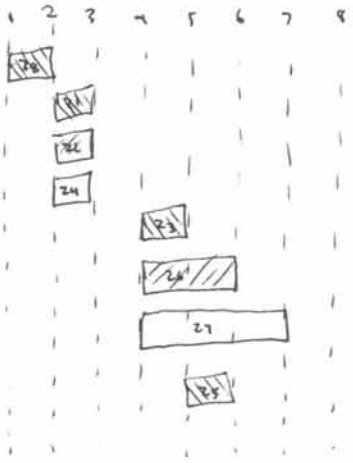
ALUs:

LEFT-EDGE coloring:

ALU1: v_{10}, v_{11}, v_4, v_5, v_9

Register sharing and Binding:

Registers:



LEFTEDGE coloring:

REG1: 28, 21, 23, 25

REG2: 22, 26

REG3: 24, 27

MULT1: v_1 (3, x) → 21

v_3 (21, 22) → 23

MULT2: v_2 (4, dt) → 22

v_7 (24, dt) → 26

MULT3: v_6 (3, y) → 24

v_8 (4, dx) → 27

ADD1: v_{10} (x, dt) → 28 (x1)

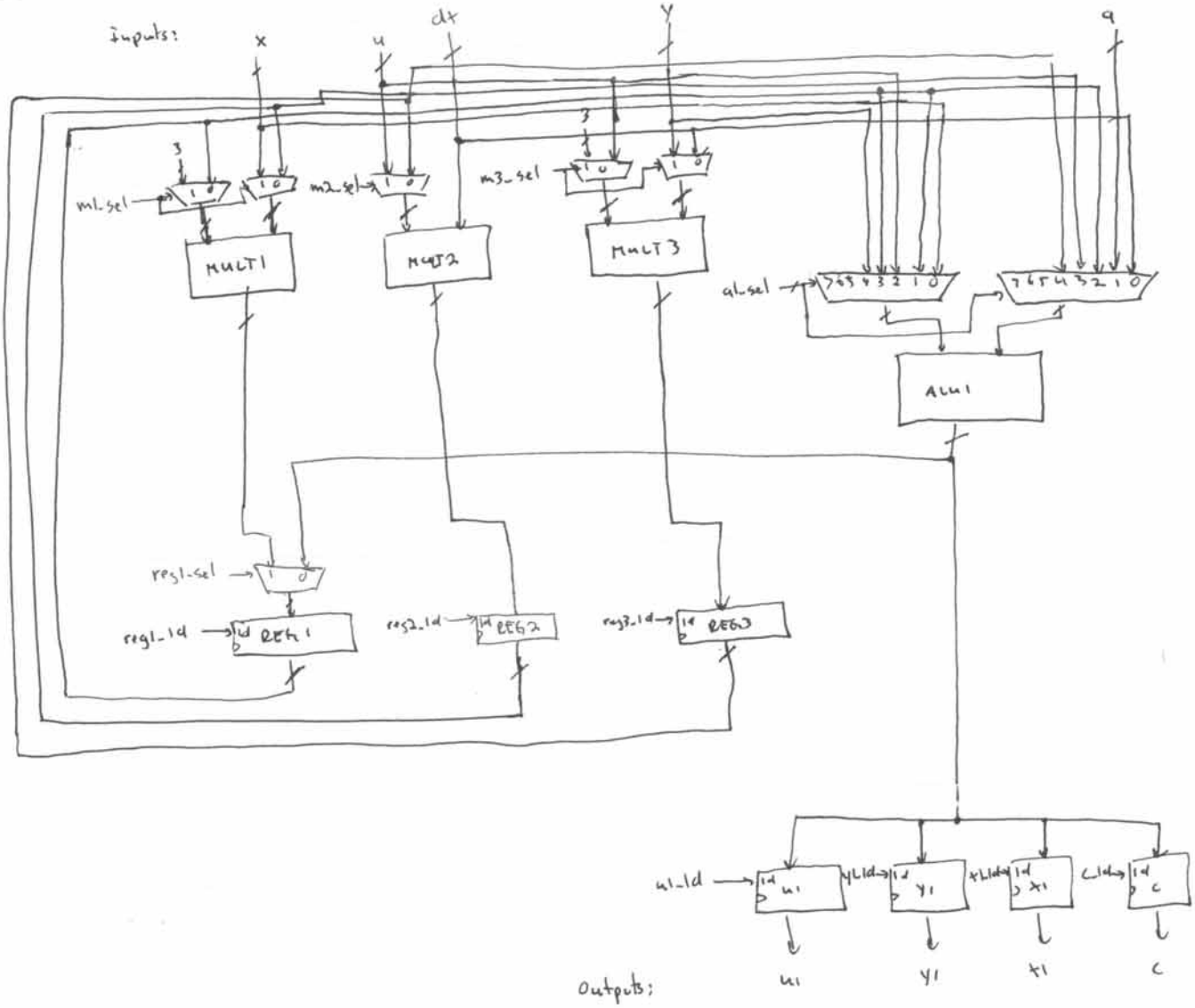
v_{11} (28, 9) → (c)

v_4 (4, 23) → 25

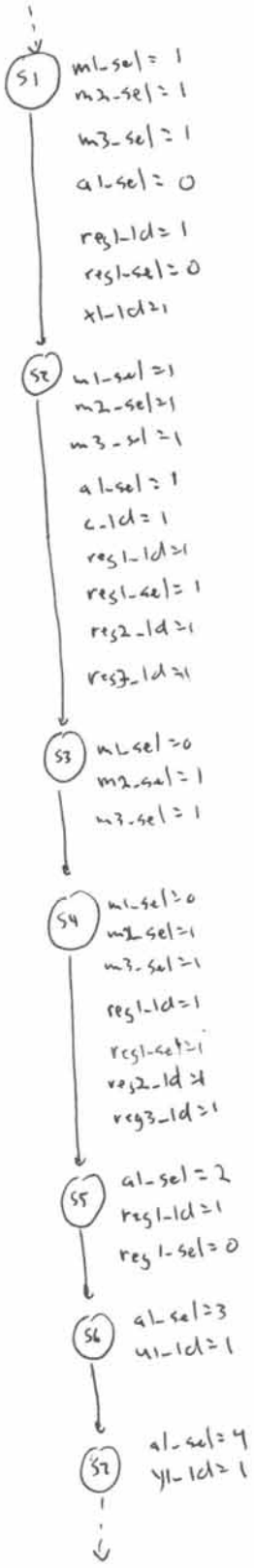
v_5 (25, 26) → (u1)

v_9 (y, 27) → (y1)

Datapath:


Inputs:
x
u
dx
y
q
m1_sel
m2_sel
m3_sel
MULT1
MULT2
MULT3
a1_sel
ALU1
reg1_sel
reg1_ld
reg2_ld
reg3_ld
REG1
REG2
REG3
u1_ld
y1_ld
x1_ld
c_ld
u1
y1
x1
c
Outputs:
u1
y1
x1
c

Controller


S1
m1_sel = 1
m2_sel = 1
m3_sel = 1
a1_sel = 0
reg1_ld = 1
reg1_sel = 0
x1_ld = 1
S2
m1_sel = 1
m2_sel = 1
m3_sel = 1
a1_sel = 1
c_ld = 1
reg1_ld = 1
reg1_sel = 1
reg2_ld = 1
reg3_ld = 1
S3
m1_sel = 0
m2_sel = 1
m3_sel = 1
S4
m1_sel = 0
m2_sel = 1
m3_sel = 1
reg1_ld = 1
reg1_sel = 1
reg2_ld = 1
reg3_ld = 1
S5
a1_sel = 2
reg1_ld = 1
reg1_sel = 0
S6
a1_sel = 3
y1_ld = 1
S7
a1_sel = 4
y1_ld = 1