## ECE 474A/57A <br> Computer-Aided Logic Design

## Lecture 6

Algorithmic State Machines (ASMs)

## What Control Path Implements?

- Sequencing of control signals to execute algorithm implemented by circuit
- Algorithm
- Finite set of instructions/steps to solve a problem
- Terminates in finite time at a known end state
- Many representations


Recipe


## Control and Datapath Interaction

- Binary information in digital system can be classified into two categories
- Data
- Discrete elements of information manipulated by arithmetic, logic, shift, and other data processing
- Operations implemented via digital components such as adders, decoders, muxes, etc
- Control
- Provides command signals that
coordinate the execution of various perations in data section to
accomplish desired task



## Flowcharts and Algorithmic State Machines (ASM)

- Flowchart
- Convenient way to graphically specify sequence of procedural steps and decision paths for algorithm
- Enumerates sequence of operations and conditions necessary for execution
- Algorithmic State Machine (ASM)
- Flowchart defined specifically for digital hardware algorithms
- Flowchart vs. ASM
- Conventional flowchart
- Sequential way of representing procedural steps and decision paths for algorithm
- No time relations incorporated
- ASM chart
- Representation of sequence of events together with timing relations between states of Representation of sequence of events together with timing relations betw
sequential controller and events occurring while moving between steps


## ASM Chart

- Three basic elements
- State box
- Decision box
- Conditional box
- State and decision boxes used in conventional flowcharts
- Conditional box characteristic to ASM


State Box


Decision Box


Conditional Box

## Decision Box

- Reflects the effect of an input
- external or internal, input or status
- Diamond shaped box
- Condition to be tested inside

- Two or more outputs represent exit paths
dependant on value tested
- In binary case one path represents true the other false, represented by 1 and 0 respectively
- Example
- Check B
- If B is true (=1), take path marked
- If $B$ is false $(=0)$, take path marked 0


## State box

- Used to indicate states in control sequence
- State name and binary code placed on top of box
- Register operations and names of output signals generated in state placed inside box

Example

- State name: S_pause
- Binary encoding: 0101
- Register operation: $\mathrm{R} \leftarrow 0$
- Register $R$ is to be cleared to 0
- Output signal asserted: Start_OP = 1
- Launches some operation in datapath



## Conditional Box

- Unique to ASM
- Inputs come from one of exit paths of decision boxes
Register operation or outputs listed insid
box generated during given state
- Generated as Mealy-type signals
- Example
- Status of input B checked
- Conditional operation executed dependin

Conditional operation executed dep
on result coming from decision bo

- If $B=1$, assert Incr_Reg signal
- Otherwise Incr_Reg remains unchanged


## ASM Block

- Structure consisting of
- One state box
- All decision and conditional boxes associated with its exit paths
- Block has one entrance and any number of exits paths
- Each block in ASM dedicated to state of system during one clock cycle
- Simplifications

- ASM Block not usually drawn because
blocks are well defined
- Can label just the " 1 " and omit the " 0 "
- ASM chart consists of one or more interconnect ASM Blocks


## ASM Example

- Convert pseudo code to ASM chart
- Example
- Want to detect the number of 1's in a 2bit register called Input
- start input indicates when to begin comparison
- busy output indicates when comparison in progress
ones hold count value
- Foutputs result

SO ${ }^{\text {busy }}=0 ;$
ones $=0 ;$
if(start $=\mathbf{1}$ )
goto
else
s1: goto so
busy $=1$;
if(lliput $[1]==1)$
ones $++;$
${ }_{\text {S2 }}{ }_{\text {busy }}^{\text {goto }} \mathbf{~ 1 ; ~}$
busy $=1 ;$
if(llnputio $==1$ )
ones $++;$
if $($ Input $[0]==$
ones $++;$
S3: ${ }^{\text {goto }}$ S3
busy $=0$;
$\mathrm{F}=$ ones
goto So

## Interpretation of Timing Operations

- Conventional flowchart, evaluation of each follows one another
- Reg A incremented
- Condition E evaluated
- If $\mathrm{E}=1$
- clear B
- Go to state S_3

In ASM the entire block considered as one unit


- All operations within block occurring
during single edge transition
- The next state evaluated during the
same clock
- System enters next state S 1, S 2, or

S 3 during transition of next clock

## ASM Example Continued



## ASM - Mux

- Describe a $4 \times 1$ MUX using a ASM

$4 \times 1$ mux



## ASM - Full Adder

- Describe a 1 -bit full adder using an ASM chart


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## Smaller Multiplier -- Sequential (Add-and-Shift) Style

- Smaller multiplier: Basic idea
- Don't compute all partial products simultaneously
- Rather, compute one at a time (similar to by hand), maintain running sum

(new running sum) 0011
0001001


## Smaller Multiplier

- Multiplier in array style
- Fast, reasonable size for 4-bit: $4 * 4=16$ partial product AND terms, 3 adders
- Rather big for 32-bit: 32*32 = 1024 AND terms, and 31 adders



Smaller Multiplier -- Sequential (Add-and-Shift) Style
Step 0
$-\quad$ Set
: Ster running sum to 0

Step 1
Mrent multiplier bit ( (mro) multificand to running sum
Shift running sum right 1 position
Step 2
-. multiplier bit $1(m r 1)$ running sun

- Shift running sum right 1 position

Step 3
Check multiplier bit $2(\mathrm{mr} 2)$
Shift running sum right 1 position
Step 4

- Check multiplier bit 3 (mr3)


ASM - Sequential Multiplier


## ASMs to FSMDs

- Able to convert between formats
- Once we have a FSMD, we've already seen how to implement in hardware


Not Used Much, But ...


