Xilinx ISE 11.1 Simulation Tutorial

This tutorial provides a step-by-step guide to simulating a Verilog description of a 2-input AND gate using Xilinx ISE 11.1 – 11.4.

- 1. Start Xilinx ISE Project Navigator
- 2. Create a new project
 - Click on File, then choose New Project on the drop down menu
 - Enter your project name, in this case the project is called "AND2gate"
 - Choose your project location, this project is stored at "Z:\Projects\AND2gate"
 - Leave the working directory entry blank.
 - Choose HDL as the source type from the Top-Level Source Type menu.
 - Click Next button

📧 New Project Wizard 🛛 🔀										
Create New Project Specify project loo										
Enter a name, locati	ions, and comment for the project									
Name:	And2gate									
Location:	C:\Temp\Projects\And2gate									
Working Directory:										
Description:										
- Select the type of to	Select the type of top-level source for the project									
Top-level source typ										
HDL										
More Info	Next >	Cancel								

- 3. You will be asked to select the hardware and design flow for this project.
 - For *Family*, choose *Spartan3E*
 - For *Device*, choose *XC3S500E*
 - For *Package*, choose *FG320*
 - For *Speed*, choose -4
 - For *Simulator*, choose *ISim (VHDL/Verilog)*
 - Click Next button

elect the device and design flow for the	Value	
Property Name Product Category		~
Family	Spartan3E	~
ramiy Device	xC35500E	~
Package	FG320	
Speed	-4	*
Top-Level Source Type	HDL	~
Synthesis Tool	XST (VHDL/Verilog)	~
Simulator	ISim (VHDL/Verilog)	~
Preferred Language	Verilog	~
Property Specification in Project File	Store non-default values only	~
Manual Compile Order		
Enable Enhanced Design Summary		
Enable Message Filtering		
Display Incremental Messages		

4. Next you are asked if you want to create new source files. We'll add source files later so just click on the *Next* button.

additional s	tionally create one source at this time. You ources with the "Project->New Source" co		: page, and later create
Create a new so	urce		
	Source File	Туре	New Source
1			Remove

5. You are asked if you want to add existing source files. Since we have a new project we don't have any existing files. Additionally, if you did have pre-existing files, you can also add these to the project later. Click on the *Next* button.

152	🖻 New Project Wizard 🛛 🛛 🔀									
¢	Add Existing Sources Adding existing sources is optional. Additional sources can be added after the project is created using the "Project- >Add Source" or "Project->Add Copy of Source" commands.									
	٨dd	existing sources								
		Source File Copy to Project	Add Source							
	1		Remove							
	Mor	re Info	Cancel							

6. A project summary will appear. Click on the *Finish* button.

🚾 New Project Wizard
Project Summary Project Navigator will create a new project with the following specifications.
Project: Project Name: And2gate Project Path: C:\Temp\Projects\And2gate Working Directory: Description: Top Level Source Type: HDL
Device: Device Family: Spartan3E Device: xc3s500e Package: fg320 Speed: -4
Synthesis Tool: XST (VHDL/Verilog) Simulator: ISim (VHDL/Verilog) Preferred Language: Verilog Property Specification in Project File: Store non-default values only Manual Compile Order: false
Enhanced Design Summary: enabled Message Filtering: disabled Display Incremental Messages: disabled
More Info < Back Finish Cancel

- 7. You now have a project by the name of "AND2gate". Next you want to specify the files in this project are for behavioral simulation.
 - Click on the Sources for: drop down menu, choose Behavioral Simulation

Choose	🚾 IS	E Proj	ect N	avigator	- C:\Ter	np\Proj	ects\Ar	nd2gate\/	nd2gat	e.xise				_	
"Behavioral	File	Edit	View	Project	Source	Process	Tools	Window	Help						
"Behavioral Simulation"	Desigr	Sources Hierarch	for B ny And2g xc3s5l No Ne Ne Ie desig	ehavioral S	iimulation	₽× • • • • •				XX	<i>P</i>	<u>-</u>	I 📭 🔢 🖋	* » :)	>> 😯
	Consc Consc	le	Files	Libraries		nd in Files								+	• = # ×

- 8. Now we want to add a new file to our project.
 - Click on *Project*, choose *New Source*
 - Choose *Verilog Module* as the file type
 - In the *File name*: box enter the desired file name, in this case the file is named "and2gate.v"
 - Click on the *Next* button

🖻 New Source Wizard 🛛 🔀								
Select Source Type Select source type, file name and its location.								
 IP (CORE Generator & Architecture Wizard) Schematic User Document Verliog Module Verliog Test Fixture VHDL Library VHDL Package VHDL Test Bench Embedded Processor 	File name: and2gate.v Location: C:\Temp\Projects\And2gate							
More Info	Next > Cancel							

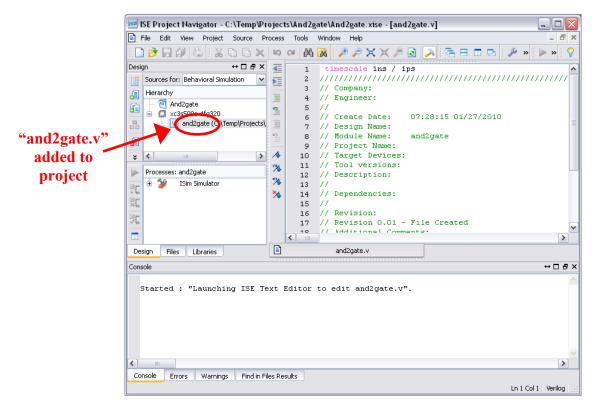
9. You will be asked for the module's port names/types. You can skip this step and click on the *Next* button.

Define Moo Specify	dule ports for module.						
1odule name	and2gate						
	Port Name	Directio	n	Bus	MSB	LSB	
		input	~				
		input	~				
		input	~				
		input	~				
		input	~				
		input	~				
		input	~				
		input	~				
		input	~				
		input	~				
		input	~				
		input	~				-

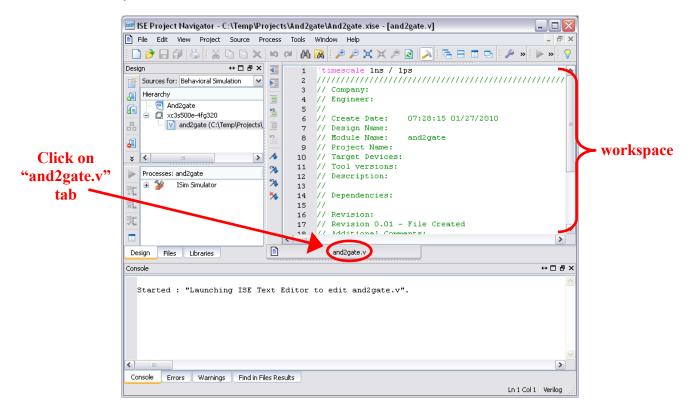
10. A project summary will appear. Click on the Finish button.

📧 New Source Wizard	×
Summary Project Navigator will create a new skeleton source wit	h the following specifications.
Add to Project: Yes Source Directory: C:\Temp\Projects\And2gate Source Type: Verilog Module Source Name: and2gate.v Module name: and2gate Port Definitions:	
More Info	< Back Finish Cancel

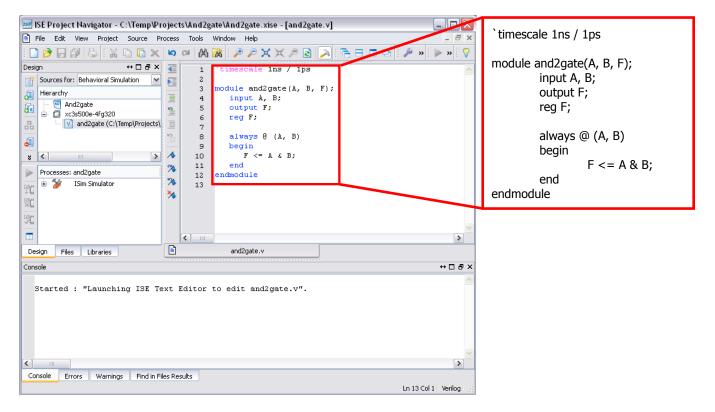
11. The "and2gate.v" file has been added to your project.



12. Click on the and2gate.v tab to show the file contents. You are now ready to specify the and2gate module's functionality.



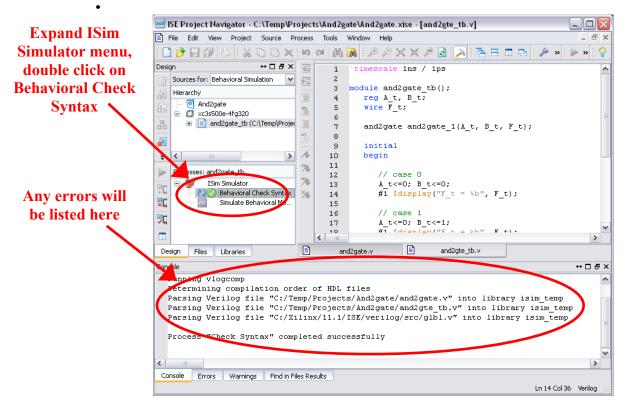
- 13. Notice that the ISE has already entered a comments sections along with a couple of lines of code for us.
 - The line "`timescale 1ns/ 1ps" is located at the top of the file. The Verilog language uses dimensionless time units, and these time units are mapped to "real" time units within the simulator. `timescale is used to map to the "real" time values using the statement `timescale <time1> / <time2>, where <time1> indicates the time units associated with the #delay values, and the <time2> indicates the minimum step time used by the simulator.
 - The and2gate module is also declared using "module and2gate();" and "endmodule", but the ports are left for us to define.
 - We finish specifying the functionality of the and2gate module as shown below.



14. We also want to add a test bench and again follow Steps 8 – 11 to add "and2gate_tb.v". Then we add the functionality of the testbench module as shown below.

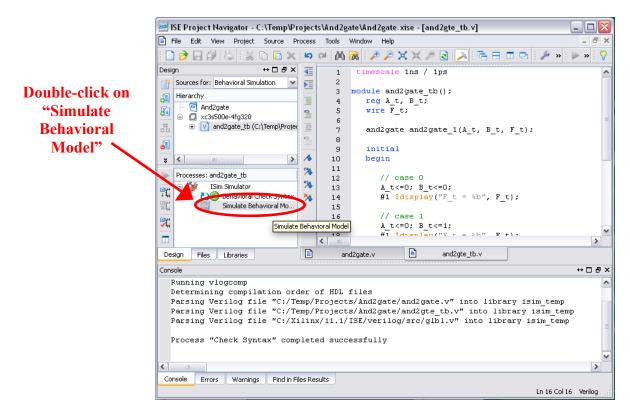
🚾 ISE Project Navigator - C:\Temp\Pr	`timescale 1ns / 1ps							
File Edit View Project Source Process Tools Window Help								
i 🗋 🆻 🗐 🕼 🕌 i 🐰 🗅 🗳 🗙	5	⊲ M	🕅 : 🎤 🔎 🗙 🗶 🔎 💽 🥕 🖻 🗖 🖻	🗄 🔑 🗴 : 🕨 : 📎	module and2gate_tb();			
Design ↔ □ ₽ ×	4 E	1	`timescale 1ns / 1ps	^	reg A_t, B_t;			
Sources for: Behavioral Simulation 💌	ÞE	2	<pre>module and2gate tb();</pre>		wire F t;			
Hierarchy		4	reg A t, B t;					
Image: Image	2	5	wire F_t;		and2gate and2gate_1(A_t, B_t, F_t);			
and2gate_tb (C:\Temp\Projec		6	and2gate and2gate $1(A t, B t, F t)$					
	2	8	analyase analyase_r(n_s, b_s, r_s,	,	1-11-1			
		9	initial		initial			
* <	A	10 11	begin		begin			
Processes: and2gate_tb	*	12	// case 0					
🛒 🕀 🎾 ISim Simulator	*	13	A_t<=0; B_t<=0; #1 \$display("F t = %b", F t);		// case 0			
	*	14 15	#1 \$display("r_t = \$b", r_t);		A t<=0; B t<=0;			
St.		16	// case 1		$\#1$ \$display("F_t = %b", F_t);			
		17	$A_t <= 0; B_t <= 1;$ $#1 Sdienler("E t = 2b", E t);$	~				
		<		>	// case 1			
Design Files Libraries		ar	nd2gate.v 📄 and2gte_tb.v		A t<=0; B t<=1;			
Console				↔□♂×	, ,			
				<u>~</u>	#1 \$display("F_t = %b", F_t);			
Started : "Launching ISE Te	xt	Editor	to edit and2gate.v".					
Started : "Launching ISE Te	xt	Editor	to edit and2gte_tb.v".		// case 2			
					A_t<=1; B_t<=0;			
					#1 \$display("F_t = %b", F_t);			
<				~	// case 3			
Console Errors Warnings Find in Fil	es De	aulta			A t<=1; B t<=1;			
Add a new source to the project	es ke	suits		Ln 12 Col 16 Verilog	$\#1 $display("F_t = \%b", F_t);$			
ride driver boards to the project				Lin in Conto , Volliog , ;	π = φ uispidy(i _t = γ 00 , i _t),			
				· · · · · · · · · · · · · · · · · · ·	and			
				<u>۱</u>	end an desa duda			
					endmodule			

- 15. After saving both "and2gate.v" and "and2gate_tb.v", we want to check the syntax of both files.
 - Expand the ISim Simulator menu, double click on Behavioral Check Syntax
 - If the syntax was correct, a checkmark appears beside the Check Syntax menu
 - If the syntax was incorrect, the window at the bottom will list the individual errors.

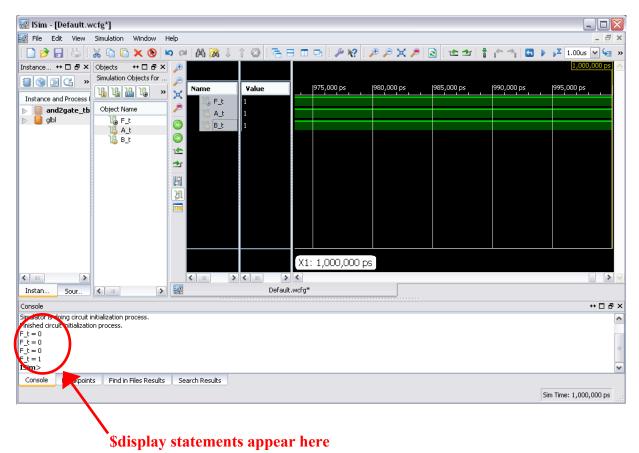


16. Now it's time to simulate the design.

• Double-click on the Simulate Behavioral Model icon

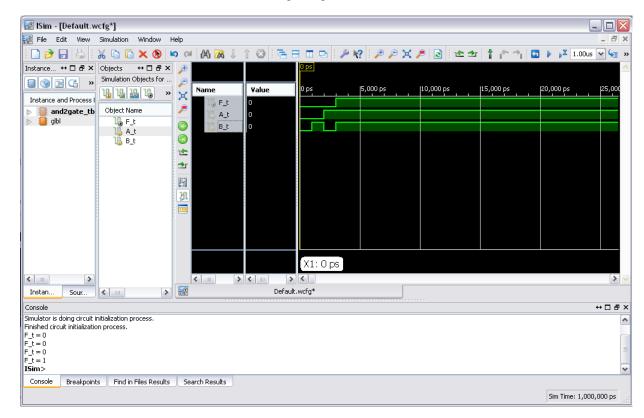


17. The ISim Simulator open in a new windows displaying a waveform and run a default simulation for some number of time units. We can now check the and2gate module's functionality. Further, the \$display statements included in the testbench appear in the lower window.

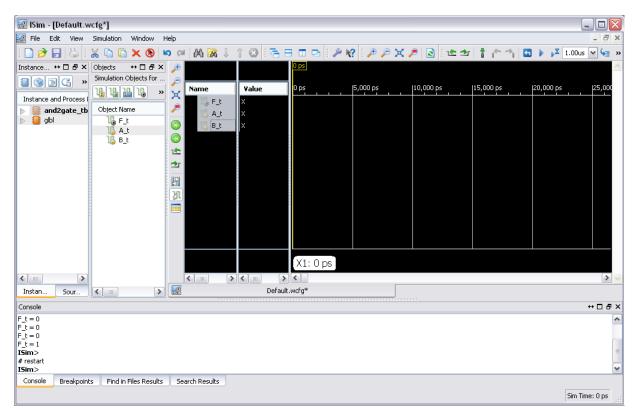


- 🔝 ISim [Default.wcfg*] _ D 🗙 **Click on** 🐖 File Edit View Simulation Window - 8 × Help 🗋 🎓 🔒 😓 🗄 🔞 🗄 🗄 🗔 🚭 🤌 🌮 🛠 🔎 😒 🕴 🛳 👘 🏫 🐴 🗳 1.000s 🗹 🧺 🕷 🔏 🗈 🛅 🗙 🛞 📁 (cil A 🕅 🕽 "Go To astance... ↔ 🗆 🗗 🗙 Objects ⇔⊡₽× Æ Time 0" » Simulation Objects for ... [G] ۶ ¥alue 975,000 ps 980,000 ps 985,000 ps |990,000 ps 995,000 ps Name ╚╚╝╝ » 🗙 Instance and Process I 🔓 F_t and2gate_tb
 glbl ۵ Object Na A_t , 10 F_t 10 A_t 10 B_t 6 B_t ΘIJ 1 ₫r 5 ય્રા X1: 1,000,000 ps < > < **>**< > < > Default.wcfg* Instan.. Sour. < Console ⇔⊡₽× Simulator is doing circuit initialization process Finished circuit initialization process. ^ $F_t = 0$ $F_t = 0$ $F_t = 0$ $F_t = 1$ **ISim**> ~ Console Breakpoints Find in Files Results Search Results Sim Time: 1,000,000 ps
- 18. To view the beginning of simulation, click on the Go To Time 0 button.

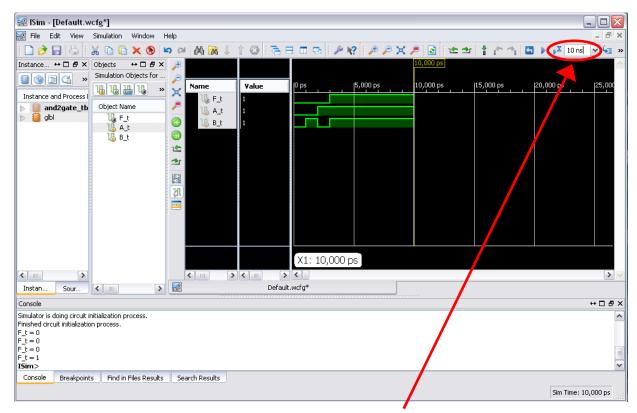
19. We can now see the simulation waveform for the beginning out our simulation.



20. To control the simulation time, we can restart the simulation and simulation for a specific length of time. Either click on the *Restart* button or select *Restart* from the *Simulation* menu. We will now have an empty waveform.



21. To simulate for a specific length of time, enter the desired simulation time and click on the *Run for the time specified in the toolbar button*. In our case, we want to simulate for 10 ns.



Enter the simulation time and click on "Run for..."