Xilinx ISE Synthesis Tutorial

The following tutorial provides a basic description of how to use Xilinx ISE to create a simple 2-input AND gate and synthesize the design onto the Spartan-3E Starter Board pictured below. This tutorial should also work with the Xilinx WebPAC that can be downloaded from Xilinx website.



- 1. Start Xilinx ISE Project Navigator
- 2. Create a new project
 - Click on File, then choose New Project on the drop down menu
 - Enter your project name, in this case the project is called "AND2gate"
 - Choose your project location, this project is stored at "C:\Temp\Projects\AND2gate"
 - Choose *HDL* as the source type from the *Top-Level Source Type* menu.
 - Click Next button

Proiect Name:	Project Location
AND2gate	C:\Temp\Projects\AND2gate
elect the Type of Top-Level Sourc	ce for the Project
HDL	· · · · · · · · · · · · · · · · · · ·
HDL	
Schematic	
NGC/NGO	

- 3. You will be asked to select the hardware and design flow for this project. *Note:* If you forget which hardware you are using, you can usually find this information printed on the FPGA.
 - For *Family*, choose *Spartan3E*
 - For *Device*, choose *XC3S500E*
 - For *Package*, choose *FG320*
 - For *Speed*, choose -4
 - For Simulator, choose ISE Simulator (VHDL/Verilog)
 - Click Next button

Project Properties		2
Property Name	Value	- 1
Product Category	All	~
Family	Spartan3E	~
Device	XC3S500E	~
Package	FG320	~
Speed	-4	~
Top-Level Source Type	HDL	~
Synthesis Tool	XST (VHDL/Verilog)	~
Simulator	ISE Simulator (VHDL/Verilog)	~
Enable Enhanced Design Summary		
Enable Message Filtering		
Display Incremental Messages		
OK Cancel	Default Help	

4. Next you are asked if you want to create new source files. We'll add source files later so just click on the *Next* button.

	New Source
Source File	Type

5. You are asked if you want to add existing source files. Since we have a new project we don't have any existing files. Additionally, if you did have pre-existing files, you can also add these to the project later. Click on the *Next* button.

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ding urce'	existing sources is optional. Additional so " or "Project->Add Copy of Source" comm	rces can be added after the project is created using the "Project->Add ands.

6. A project summary will appear. Click on the *Finish* button.

Project Navigator will cr	eate a new project with the following specifications:	
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Device:	xc3s500e	
Package:	ft256	
Speed:	-5	
Synthesis 1	ool: XST (VHDL/Verilog)	
Simulator:	ISE Simulator (VHDL/Verilog)	
Enhanced De	sign Summary: enabled	
Message Fil	tering: disabled	

- 7. You now have a project named "AND2gate". Next you want to add or create files for this project that will be synthesized onto the Spartan3 Starter Board. However, new files added to your project will be added as simulation files. Use the following steps to add a new file to your project.
 - Click on the *Sources for*: drop down menu, choose "Behavioral Simulation"

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- 8. Now we want to add a new file to our project.
 - Click on *Project*, choose *New Source*
 - Choose *Verilog Module* as the file type
 - In the *File name:* box enter the desired file name, in this case the file is named "and2gate.v"
 - Click on the *Next* button

New Source Wizard - Select Source Type (P (Coregen & Architecture Wizard) Schematic State Diagram Test Bench WaveForm User Document Verlog Module Worlog Test Fixture VHDL Module P VHDL Library P VHDL Package	Pe
More Info	Add to project Add to project Cancel

9. You will be asked for the module's port names/types. While you can use this dialog to create the port names, we will manually add them later within the Verilog file itself. You can skip this step and click on the *Next* button.

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10. A summary will appear. Click on the Finish button.

Mew Source Wizard - Summary	_ 🗆 🔀
Project Navigator will create a new skeleton source with the following specifications:	
Add to Project: Yes Source Directory: C:\Temp\Projects\and2gate Source Type: Verlog Module Source Name: and2gate v Module Name: and2gate Port Definitions:	
< Baok	inish Cancel

• The "and2gate.v" file has been added to your project.



11. Click on the "and2gate.v" tab to show the file contents. You are now ready to specify the and2gate module's functionality.



12. Notice that the ISE has already entered a couple of lines of code for us.

- The line "`timescale 1ns/ 1ps" is located at the top of the file. The Verilog language uses dimensionless time units, and these time units are mapped to "real" time units for simulation. `timescale is used to map to the "real" time values using the statement `timescale <time1> / <time2>, where <time1> indicates the time units associated with the #delay values, and the <time2> indicates the minimum step time used by the simulator.
- The and2gate module is also declared using "module and2gate();" and "endmodule", but the ports are left for us to define.
- We finish specifying the functionality of the and2gate module as shown below.



- 13. We now want to synthesize the AND2 gate circuit onto the Spartan3E Starter Board. While we will skip to synthesis in this tutorial, it is always a good idea to first simulate the design to ensure correctness.
 - Right click on the and2gate (and2gate.v) in the *Sources* area and select *Properties*.

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• Choose *Synthesis/Imp* + *Simulation* as the file association

this dialog to cha	nge the source views that the design unit appears in.	
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• Click on the *Sources for*: drop down menu, choose "Synthesis/Implementation"

Xilinx - ISE - C:\Temp\Projects\AND2gate\AND2gate.ise - [and2gate.v*]	
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8 always () or B)	
9 begin	
10 F <= A 4 B;	
12 endmodule	
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Click on the and2gate (and2gate.v) in the Sources area. •



14. Before we synthesize our design, we need to map the and2gate's inputs and outputs to the pins of the FPGA that we want connected to our design using a User Constraint File (UCF). For this circuit we will use the two of the switches on the Spartan3E Starter Board as the inputs (A, B) and one of the LEDs as the output (F). The following picture show which switches and LED we will be using. Printed on the board next to each of the components is the pin number associated with that component.



• Expand the User Constraints by clicking on the + symbol located to the left.



- Double-click on *Edit Constraints*.
- You will be asked if you want to create an Implementation Constraint File (UCF). Choose Yes.
- A new file named "and2gate.ucf" will be created and added to your project.
- We specify the connection between out and2gate design and the FPGA's pins as shown below. Be sure to save the UCF file before proceeding.



- 15. We can now synthesize our design.
 - Click on the and2gate (and2gate.v) in the *Sources* area.

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• Double-click on *Synthesize – XST*. This step will synthesize your design to the basic logic structures of the FPGA (LUTs). When completed, you should hopefully see a message *Process "Synthesize" completed successfully*. If not, please go back and make sure you followed the previous steps correctly.

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8 always @ (A or B)	
9 begin	
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11 end	
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• Double-click on *Implement Design*. This step will perform technology mapping, placement, and routing to create a final implementation for your design. When completed, you should hopefully see a message *Process* "*Generate Post-Place & Route Static Timing*" completed successfully. If not, please go back and make sure you followed the previous steps correctly.

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	8 always @ (A or B)	
	9 begin	
	10 F C A & B;	
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• Double-click on *Generate Programming File*. This step will create the bitstream that we will use to program the FPGA on the Spartan3E Starter Board. When completed, you should hopefully see a message "*Generate Programming File*" completed successfully. If not, please go back and make sure you followed the previous steps correctly.



- 16. We are now ready to program the Spartan3E Starter Board. You should be as <u>careful as possible</u> when using these FPGA development boards. If you need to unplug the power, please <u>wait 30 seconds</u> before plugging the power supply in again. This will help to ensure a long life for the board.
 - Plug the power supply into an appropriate wall socket.
 - Plug the power supply into the Spartan3 starter board.
 - Connect the Spartan3 Starter Board to the USB port of your computer using the supplied programming cable.
 - Connect the other end of the supplied cable to Spartan3 Starter Board at the location shown below.
 - Make sure your board is "ON", a light should illuminate by the power supply if the board is on.





USB Type B Connector - Connects to Starter Kit's USB connector

USB Type A Connector Connects to computer's USB connector



17. Expand the Generate Programming File by clicking on the + symbol located to the left.

Zilinx - ISE - C:\Temp\Projects\AND2gate\AND2gate.ise - [and2gate.ucf]	
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Generate PROM. ACE, or JTAG File	
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- Double-click on *Configure Device (iMPACT)*. This will launch the iMPACT tool that we will use to program the FPGA. *Note: It may take a few minutes for the program to launch the first time. Please be patient.*
- You will be prompted to select what you would like to do. Choose *Configure Device using Boundary-Scan* (*JTAG*) and make sure *Automatically connect to cable and identify Boundary-Scan* is selected. Click *Finish*.

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Please select an action fro	m the list below
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Automatically	connect to a cable and identify Boundary-Scan chain
O Prepare a PROM File	
O Prepare a System AC	E File
O Prepare a Boundary-S	Scan File
	SVF 💌
O Configure devices	
	using Slave Serial mode
	< Back Finish Cancel

• You will be prompted to Assign a New Configuration File. This file is for the Spartan3E FPGA we are configuring. Choose the and2gate.bit file in the Z:/Projects/AND2gate directory. Click *Open*.

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• The following warning will be displayed. Click *OK*.

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	WARNING: MPACT: 2257 - Startup Clock has been changed to 'JtagClk' in the bitstream stored in memory, but the original bitstream file remains unchanged.
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• You will again be prompted to Assign a New Configuration File. This file is for the FLASH memory that can be used to store the FPGA configuration. We will not be using the FLASH at this time. Click *Bypass*.

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• You will again be prompted to Assign a New Configuration File. This file is for the CPLD. We will not be using the CPLD at this time. Click *Bypass*.

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• Right click on the device labeled xc3s500e and choose Program...



• You will be presented with the Programming Properties. Click OK.

egory	
 Programming Properties Advanced PROM Programming Properties Revision Properties 	Programming Properties General Programming Properties
	Verfy
	General CPLD And PROM Properties
	Erase Before Programming Read Protect
	Prom/CoolRunner-II Usercode (8 Hex Digits)
	CPLD Specific Properties
	Write Protect Functional Test On-The-Fly Program
	XPLA UES Enter up to 13 characters
	PROM Specific Properties
	Load FPGA Parallel Mode Use D4 for CF
	Virtex-II/Virtex-4 Programming Properties
	Pulse PROG Secure Mode Program Key

• As the FPGA is being programmed, you will see a progress dialog as shown below.



• Upon programming the FPGA you should hopefully see the *Programming Successful* message as shown below.

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• If instead you receive a *Programming Failed* message as shown below, try the following steps to correct the problem.

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MPACT Process Operations	
<pre>x '1': Programmed successfully. PROGRESS_END - End Operation. Elapsed time = 1 sec. Compared time = 1 Ultout from Warmin = 0 Ultout from Warmin = 0 </pre>	>
Ready Configuration Platform Cable USB	6 MHz usb-hs

- Remove power from the Spartan3 Starter Board by carefully unplug the power supply from the board.
- *Wait 30 seconds* and apply power by carefully plugging the power supply into the board.
- Program the device again.
- 18. Congratulations. You have successfully synthesized and implemented your 2-input AND gate onto the Spartan3E Starter Board. You can test your AND gate by changing the input switches. When both switches are enabled (in the up position) the LED should illuminate. For all other switch configurations, the LED will be off.