## ECE 274 Digital Logic

Datapath Components - Shifters, Comparators, Counters, Multipliers

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## Digital Design

Chapter 4:
Datapath Components
Slides to accompany the textbook Digital Design, First Edition,
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http:/www.ddvahid.com


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Datapath Components
Shifter Example: Temperature Averager

- Four registers storing a history of temperatures
- Want to output the average of those temperatures
- Add, then divide by four
- Same as shift right by 2
$\square$ Use three adders, and right shift by two



## Datapath Components

Barrel Shifter

- A shifter that can shift by any amount
- 4-bit barrel left shift can shift left by 0 , 1,2 , or 3 positions
- 8-bit barrel left shifter can shift left by $0,1,2,3,4,5,6$, or 7 positions (Shifting an 8 -bit number by 8 positions is pointless -- you just lose all the bits)
 mux solution for 8 -bit barrel shifter: too many wire
- Could design using $8 \times 1$ muxes and lots shift by $^{5}$ ? of wires
- Too many wires
- More elegant design
- Chain three shifters: 4, 2, and 1
- Can achieve any shift of $0 . .7$ by enabling the correct combination of those three shifters, i.e., shifts should sum to desired amount


Net result: shift by $5: 8 \downarrow_{Q} 11000000$ (by 1)

## Datapath Components

## Comparators

- N-bit equality comparator: Outputs 1 if two N -bit numbers are equal
- 4-bit equality comparator with inputs A and B
- a3 must equal b3, a2 = b2, a1 = b1, a0 = b0
. Two bits are equal if both 1 , or both 0
- eq $=\left(a 3 b 3+a 3^{\prime} b 3^{\prime}\right) *\left(a 2 b 2+a 2^{\prime} b 2^{\prime}\right) *\left(a 1 b 1+a 1^{\prime} b 1^{\prime}\right) *\left(a 0 b 0+a 0^{\prime} b 0^{\prime}\right)$
- Recall that XNOR outputs 1 if its two input bits are the same

$0110=0111 ?$



## Datapath Components

Magnitude Comparator

- By-hand example leads to idea for design
- Start at left, compare each bit pair, pass results to the right

Each bit pair called a stage

- Each stage has 3 inputs indicating results of higher stage, passes results to lower stage



## Datapath Components

Magnitude Comparator


Each stage:

- out_gt $=$ in_gt $+\left(\right.$ in_eq $\left.* a * b^{\prime}\right)$
$\mathrm{A}>\mathrm{B}$ (so far) if already determined in higher stage, or if higher stages equal but in this stage $\mathrm{a}=1$ and $\mathrm{b}=0$
- out_It = in_lt + (in_eq * $\mathrm{a}^{*}$ b)
$\mathrm{A}<\mathrm{B}$ (so far) if already determined in higher stage, or if higher stages equal but this stage $a=0$ and $b=1$
- out eq = in eq * (a XNOR b)
$\circ A=B$ (so far) if already determined in higher stage and in this stage $a=b$ too - Simple circuit inside each stage, just a few gates (not shown)

Datapath Components
Magnitude Comparator Example: Minimum of Two Numbers

- Design a combinational component that computes the minimum of two 8 -bit numbers


## Datapath Components

Counters
o N-bit up-counter: N-bit register that can increment (add 1) to its own value on each clock cycle

- 0000, 0001, 0010, 0011, ...., 1110,


$$
1111,0000
$$

- Note how count "rolls over" from 1111 to 0000

Terminal (last) count, tc, equals1 during value just before rollover

## - Internal design

$\square$ Register, incrementer, and N-input AND gate to detect terminal count


## Datapath Components

Down-Counter

○ 4-bit down-counter
ㅁ 1111, 1110, 1101, 1100 0011, 0010, 0001, 0000, 1111,
$\square$ Terminal count is 0000

- Use NOR gate to detect
- Need decrementer (-1) design like designed incrementer



## Datapath Components

Up/Down-Counter

- Can count either up or down
- Includes both incrementer and decrementer
- Use dir input to select, using $2 \times 1$ : dir=0 means up
$\square$ Likewise, dir selects appropriate terminal count value



## Datapath Components

Counter with Parallel Load

- Up-counter that can be loaded with external value
- Designed using $2 \times 1$ mux Id input selects
incremented value or external value
- Load the internal register when loading external value or when counting



## Datapath Components

4.7

## Datapath Components

Counter with Parallel Load

- Useful to create pulses at specific multiples of clock
- Not just at N -bit counter's natural wrap-around of $2^{\mathrm{N}}$
- Example: Pulse every 9 clock cycles
- Use 4-bit down-counter with parallel load
- Set parallel load input to 8 (1000)
- Use terminal count to reload

When count reaches 0 , next cycle loads 8.

- Why load 8 and not 9 ? Because 0 is included in count sequence:
$\circ 8,7,6,5,4,3,2,1,0 \rightarrow 9$ counts


Multipliers - Array Style

- Can build multiplier that mimics multiplication by hand - Notice that multiplying multiplicand by 1 is same as ANDing with 1

$$
\begin{array}{cl}
0110 & \text { (the top number is called the multiplicand) } \\
0011 & \text { (the bottom number is called the multiplier) } \\
0-110 & \text { (each row below is called a partial product) } \\
0110 & \begin{array}{l}
\text { (because the rightmost bit of the multiplier is } 1 \text {, and } 0110 * 1=0110 \text { ) } \\
0000
\end{array} \\
\text { (because the second bit of the multiplier is } 1 \text {, and } 0110 * 1=0110 \text { ) } \\
+0000 & \text { (because the leftmost bit of the multiplier is } 0 \text {, and } 0110 * 0=0000 \text { ) } \\
00010010 & \text { (the product is the sum of all the partial products: } 18 \text {, which is } 6 * 3 \text { ) }
\end{array}
$$

Datapath Components
Multipliers - Array Style

- Generalized representation of multiplication by hand

|  |  | $\times$ | $\begin{aligned} & \text { a3 } \\ & \text { b3 } \end{aligned}$ | $\begin{aligned} & \text { a2 } \\ & \text { b2 } \end{aligned}$ | $\begin{aligned} & \text { a1 } \\ & \text { b1 } \end{aligned}$ | $\begin{aligned} & \text { a0 } \\ & \text { b0 } \end{aligned}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | b0a3 | b0a2 | b0a1 | b0a0 | (pp1) |
|  |  | bla3 | b1a2 | b1a1 | b1a0 | 0 | (pp2) |
|  | b2a3 | b2a2 | b2a1 | b2a0 | 0 | 0 | (pp3) |
| + b3a3 | b3a2 | b3a1 | b3a | 0 | 0 | 0 | (pp4) |
| p7 p6 | p5 | p4 | p3 | p2 | p1 | p0 |  |

Datapath Components
Multipliers - Array Style


## In-class Exercise

Design a somewhat accurate Celsius to Fahrenheit converter.

- The conversion circuit receives a digitized temperature in Celsius as a 16-bit binary number $C$ and outputs the temperature in Fahrenheit as a 16 -bit output $F$ using the following approximation:
ㅁ $\mathrm{F}=\mathrm{C}^{*} 30 / 16+32$.

