ECE 274 - Digital Logic

Lecture 23

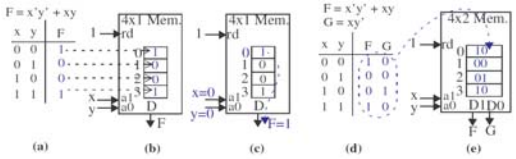
- Lecture 23 – Implementation
  - Field Programmable Gate Arrays (FPGAs)
  - Programmable Logic Devices (PLDs)

Programmable ICs

- *FPGAs – Field Programmable Gate Arrays*
  - Prefabricated ICs that contain all of the transistors and wires
  - Designer can program the FPGA to implement our desried circuit
    - Programming refers to downloading a series of bits to the FPGA's memory
    - Fast - Progamming typically takes seconds to minutes

FPGAs – Field Programmable Gate Arrays

- Lookup Tables
  - Memory used to implement a combinational circuit
  - A *1-bit* wide memory with *N* address lines (2^N words) can implement any Boolean combinational function of *N* variables



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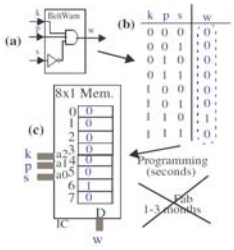
Field Programmable Gate Arrays



Lookup table implementation.

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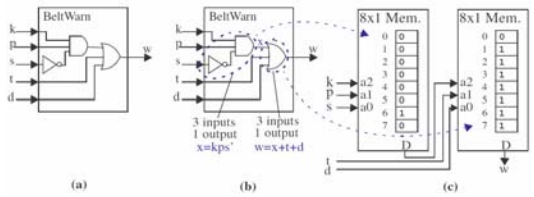
Field Programmable Gate Arrays



Partitioning a circuit onto two lookup tables: (a) desired circuit, (b) circuit partitioned into groups with at most 3-inputs and 1-output, (d) groups mapped to two 3-input 1-output lookup tables.

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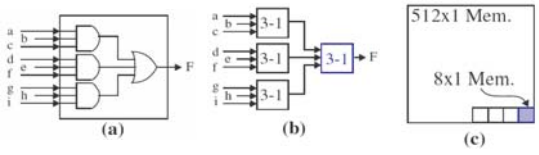
Field Programmable Gate Arrays



Dividing a many-input circuit among smaller lookup tables reduces total lookup table size: (a) 9-input circuit, (b) circuit mapped to 3-input 1-output lookup tables, (c) size savings compared to 9-input 1-output lookup table.

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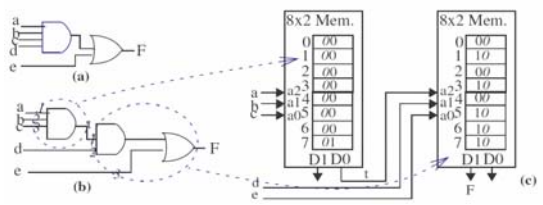
Field Programmable Gate Arrays



Partitioning a circuit onto two lookup tables: (a) original circuit, (b) transformed circuit that breaks the 4-input AND gate into two smaller gates, and then that shows the 3-input 1-output groupings, (c) mapping of each group to a lookup table, with the group's function converted to programmed bits in the lookup table. Italicized bits are unused.

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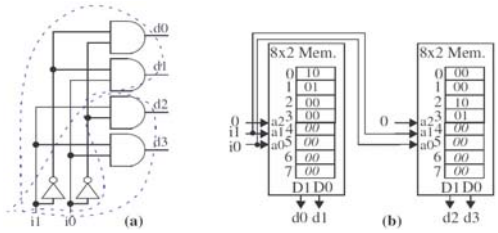
Field Programmable Gate Arrays



Mapping a 2x4 decoder to two 3-input 2-output lookup tables: (a) desired circuit, (b) mapping to two lookup tables. Italicized bits are unused.

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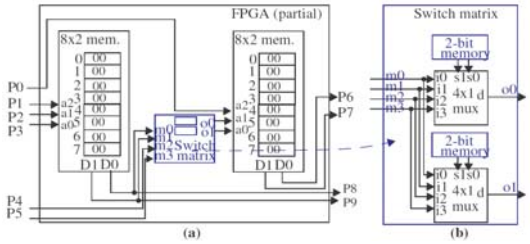
Field Programmable Gate Arrays



A simple FPGA architecture: (a) an FPGA that includes a switch matrix, and (b) the switch matrix's internals showing two 4x1 muxes controlled by two 2-bit registers. Note: real FPGAs have hundreds of lookup tables and switch matrices, not just a few.

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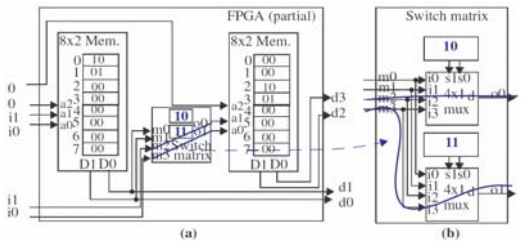
Field Programmable Gate Arrays



Implementing a 2x4 decoder on the FPGA fabric having a switch matrix: (a) external connections and programmed bits in the lookup tables and switch matrix, and (b) a look inside the switch matrix, showing the programmed connections between the outputs and inputs.

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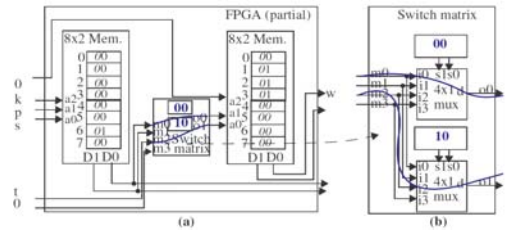
Field Programmable Gate Arrays



Implementing the extended seatbelt warning light circuit on the FPGA fabric having a switch matrix: (a) external connections and programmed bits, (b) a look inside the switch matrix, showing the programmed connections. Italicized bits in the lookup tables are unused.

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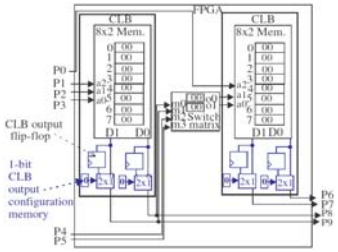
Field Programmable Gate Arrays



An FPGA with configurable logic blocks, which contain flip-flops along with a lookup table.We've put 0s in all the configuration memory bit cells in the figure.

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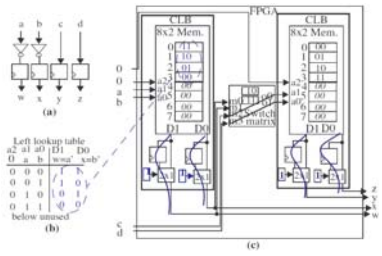
Field Programmable Gate Arrays



Implementing a sequential circuit on an FPGA: (a) desired sequential circuit, (b) left CLB's lookup table program bits, (c) programmed FPGA. Unused bits are italicized.

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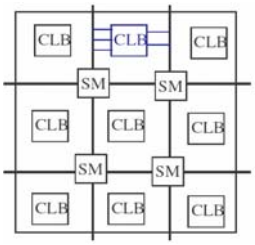
Field Programmable Gate Arrays



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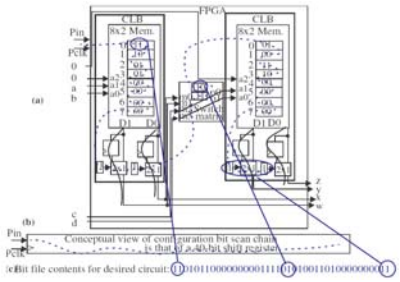
Field Programmable Gate Arrays



Programming an FPGA: (a) all configuration bit cells exist in a scan chain, (b) a scan chain conceptually is a big shift register, (c) a bit file's contents would be shifted in during programming

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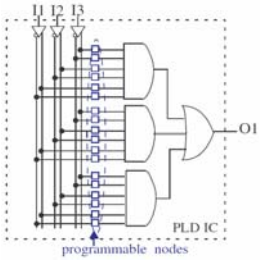
Programmable Logic Device



A basic example of a programmable logic device. (AND gates are wired-AND).

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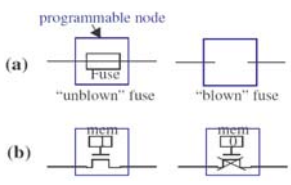
Programmable Logic Device



Two types of programmable nodes: (a) fuse based, (b) memory based.

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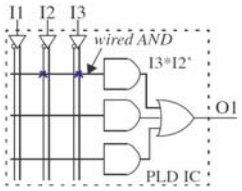
Programmable Logic Device



Simplified PLD drawing.

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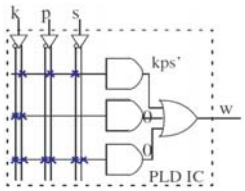
Programmable Logic Device



Seat-belt warning system on a simple PLD.

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Physical Implementation

Technology	%
Standard cell	55%
Gate array	5%
System-on-a-Chip	30%
Full-custom	10%
CPLD/FPGA	10%
Other	5%

Sample % of new implementations in various technologies. Total is more than 100% due to overlap among categories. Source: Synopsys, DAC 2002 panel.

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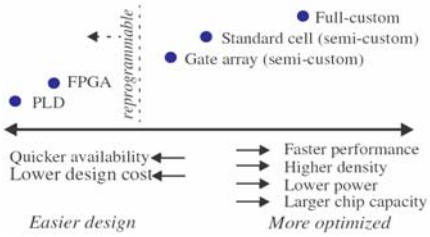
Physical Implementation



Tradeoffs among several IC technologies.

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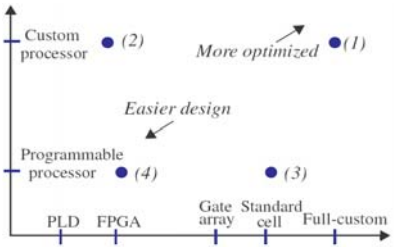
Physical Implementation



IC technologies and processor varieties are orthogonal implementation features. Four of the ten possible choices are shown.