ECE 407/507 DESIGN PROJECT

PROJECT GUIDELINES

- Load Sharing
  - Inverter
  - NOR2
  - NAND2
  - XOR
  - PARITY GENERATOR
  - SYNDROME GENERATOR
  - ENCODER
  - DECODER

- **Layout**

The layout of the Standard cells must be of **MINIMUM** in area in order to reduce the power dissipation. Make sure that you follow "good" layout practices like checking for the drc errors. Also see that your layout should be symmetric. Try to minimize the size of the final layout.

- **PSpice Analysis**

You need to do your simulations in PSpice(windows) or Spice(on UNIX machines). All the parameters which you require are given in the website:

http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/tsmc-025/n94s-params.txt

You also need to extract each of the layout in order to get the actual capacitances. If you are doing your simulations in PSpice you need to use these capacitances as explicit capaciances connected to the MOSFET. In case of spice you need to construct a cir file which includes the models, parameters and the modle files for your simulations. If you have any question about how to use these you can contact any of the TA either personally or by email.

- **Capacitance Calculation**

You need to calculate all capacitances using the hand calculations. See the text book (Uymera) for some examples. Using these capacitances and resistances you need to make a RC model of each building block.

- **Switching Times**

You should use these RC models of the building blocks to build the bigger blocks. Use these models to calculate the rise time, the fall time and others delays.

INTERIM REPORT

The Interim Project reports are due on **March 21st 2002**. You need to include the following in your Interim Project Report

- Paper/Pencil Design
- DC analysis of the building blocks
- Layout of building blocks.
- Capacitance calculations
- Transient analysis
- Speed
- Comments about the overall layout, Simulations and Hand calculations.

FINAL REPORT

Your report should include the following information:

1) A short introduction (one page maximum) about the objective and goals of the design project. You should use this introduction as a means of providing a casual reader (i.e. an engineer who has not taken this class) with a brief synopsis of your work.

2) A brief design methodology for each building block, e.g. what sort of circuit topology was chosen, and why? Include a simple RC timing analysis of each cell to demonstrate the frequency at which these cells are working.

3) A circuit schematic (including device widths and lengths) of each standard cell.

4) PSpice/Spice transient simulations to demonstate the rise and fall time, propagation delays etc. In addition to your PROBE plots, you should include a PSpice/Spice output listing (with your circuit netlist) for each standard cell.

5) In your final section, discuss the differences between your hand calculations and your simulations. And you comments about these results.

Include a table showing percentage errors between your simulation results and your hand calculations. Also be sure to include a table giving the area of each cell (determined using the box command in MAGIC) in square lambda and square microns, and calculate the sum of all areas for all of your layouts.

Keep your report concise! With the exception of drawings and plots, the written portion of your report should be 15 pages maximum. Your report does not have to be typed, but it must be neat, well organized, and have good grammar and spelling. All pages should be numbered, with explanatory titles or headings provided for all plots, drawings, and tables. (Consult any IEEE journal publication for an example of good technical formatting.)

On the cover page of your report, list the names of all group members. In addition, list the percentage effort that each group member provided to the overall design effort. (The percentage efforts should sum to 100%.) Your complete report should be placed in a three ring or edge binder or cover, with no loose sheets. Stapled reports will not be accepted - use a proper binder, please!

Due Date

Your report is due on April 23, 2002, to be turned in to the professor in class .

Late reports will be accepted with a 25% per day penalty. Your MAGIC files should be sent to the following email address with subject as **ECE 407/507 Project**.

ece507@ece.arizona.edu.

Note: All the standard cells and the final circuit should be sent in the same email.