MIXED SIGNAL ANALOG/DIGITAL BOARD

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ABSTRACT

Mixed-signal circuits are increasingly utilized in many applications, especially in communication systems. Analysis and design of such circuits is very complex. Software support tools for analysis, simulation, and design are in development. Availability of programmable analog and digital devices have brought the idea of construction a development board for mixed signal circuits. Such a board could be used for fast prototyping, experimental studies, verification of models etc. This article will explain the design of a mixed signal development board, its hardware and integrated software, carried out at the Center for Low Power Electronics at the University of Arizona in cooperation with Western Design Center (WDC). The major components used in the design are the Motorola's field programmable analog array (MPA020) and WDC microprocessor development board.

1. INTRODUCTION

The mixed-mode systems synthesis creates the problem of designing the control logic for switching the analog and digital parts of the system in accord with the timing resulting from the system specification. The analog part of the system can be realized in the ASIC technology through implementation of established analog-digital functions for signal processing technology (e.g. a/c, c/a, f/v conversion, multiplexing, programmable gain control, PLL, VCO, audio, radio, automotive circuits) as described in (National Semiconductor 1993; Siliconix 1997). An alternative to this approach is provided by Field Programmable Analog Array (FPAA) technology introduced by Motorola (Anderson *et al*. 1997; Motorola 1997). This technology gives basis for rapid prototyping of circuits, which simplifies and speeds-up the design/development process.

2. MIXED SIGNAL BOARD

Today, high demand for programmable devices in the digital area as well in analog one increases the need for mixed-mode development environment. The designers of mixed-signal circuits face many difficulties delaying the creation of final product. To speed up this process the rapid prototyping tool providing digital and analog programming abilities should be created. The creation of Mixed Signal Development System will meet these demands filling the gap in modern designs.
The project concentrates on 3 fields:
1. Design and creation of a mixed-signal development board.
2. Design and generation of integrated MS-Windows software providing necessary utilities for programming the board.
3. Design and generation of 6502 processor routines required for programming the FPAA chip and utilization of Filter Banks.
The Motorola FPAA (Field Programmable Analog Array) has been employed to perform programmable analog design generation with switched capacitor technique. The FPAA chip is a programmable analog device consisting of 20 programmable cells. The Western Design Center W65C02DB Board is utilized as a base-board providing necessary support for development of the daughter board with the FPAA chip. The WDC W65C02DB board is a stem structure of the Mixed-Signal Development Board and its microprocessor is a digital-controlling unit of the system while the Motorola FPAA chip provides easy programming facility in the analog realm.
The Figure 1 presents the communication scheme between system components.
The generation of the programming algorithm for the FPAA chip is essential. This algorithm however to be completed needs creation of a specialized PC Extension Board which can provide necessary information considering programming sequence of the FPAA chip. The PC Extension Board will also be used for checking the algorithm in practice before implementing it in 6502 microprocessor assembler language.
Once the algorithm is found and tested the development of the MS Windows software and 6502 routines can begin.

The routines for programming the FPAA from W65C02DB Board in first stage will be downloaded with utilization of the WDC Debugger and tested. For the MS Windows software (ADB Project Manager) a special technique will be develop to communicate with external programs and to communicate with software providing communication with the WDC Board. Own design structures for Filter Banks will be introduced and implemented both in the MS Windows environment and on WDC W65C02DB Board. Once the software is tested with the PC Extension Board, the daughterboard for FPAA chip will be designed and constructed. Finally all components of the project will be integrated and full programming capability achieved.

The work includes development of the project the main areas such as:

1. Extension and testing of the ADB Project Manager
2. The Compiler error files syntax analysis
3. Testing of the 6502 FPAA programming algorithm
4. WDC Board 6502 code Filter Banks implementation
5. Daughter Board design
6. FPGA daughter board design

Development of novel technique utilized for programming the Motorola FPAA chip will be necessary.

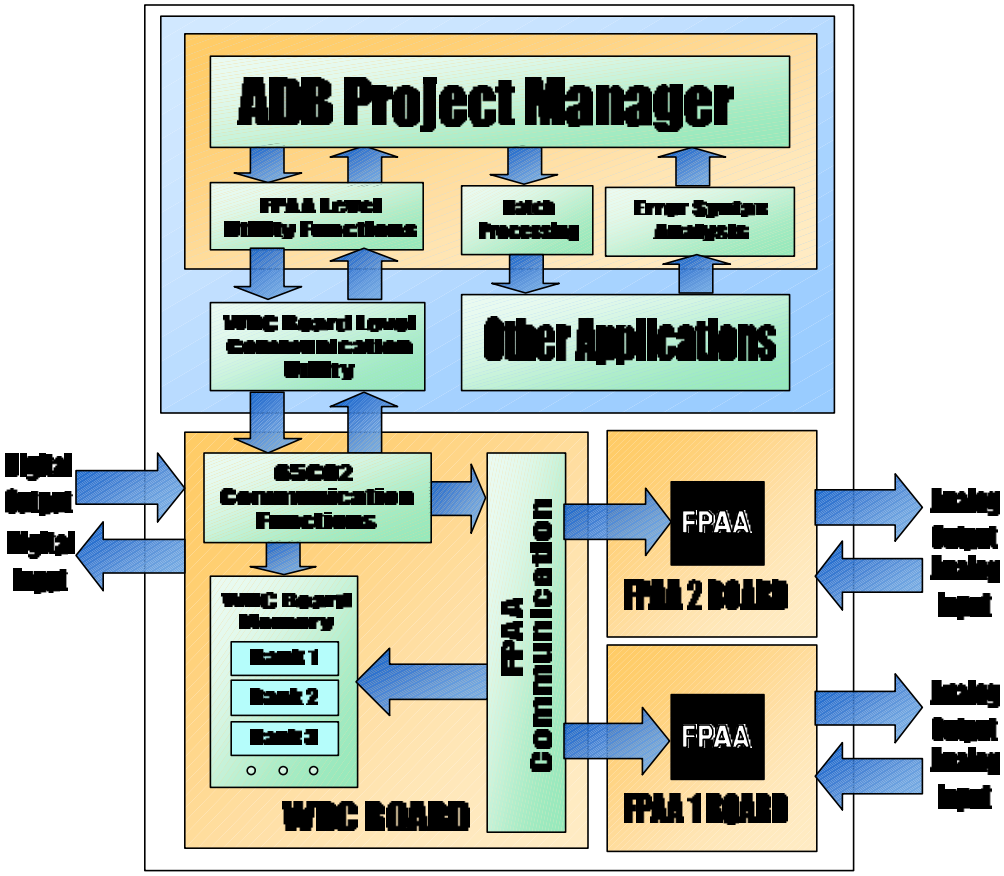

Figure 1. Block diagram of analog-digital development system.

Development of Filter Bank structures and their software implementation will be an important component of the system.

Important software components:
a) new multilevel communication scheme employed to utilize programming of multi chip FPAA structures.
b) development of the user-friendly software (ADB Project Manager) integrating into one environment several standalone programs.

The applications included: WDC Development Board programming utilities, FPAA Board (EasyAnalogTM), FPGA Board (XILINX)*, external compilers and linkers, Specialized programs (Easy Filter)

Key Accomplishments:
Design and creation of PC Extension Board,
Generation of FPAA programming algorithm,
Creation of MS Windows ADB Project Manager Application,
Development of Filter Bank structures.

3. ADB PROJECT MANGER

This is the main application of the **ANALOG/DIGITAL Board**. The program allows for creation of projects, which can consist of either 65C02 Assembly and C files or data for the FPAA connected to the WDC Board. The project can automate the process of 6502 code creation.

Parameters, which are set in the program allow for easy manipulation of files and directories as well as direct programming of FPAA and WDC board (Fig. 2).

Primary experiments that will be performed using this system include adaptive filtering with two or more FPAA's operating in parallel, and investigation of switching effects on overall performance of the adaptive filter. The switching is controlled by an external digital signal, which is processed by FPGA or microprocessor

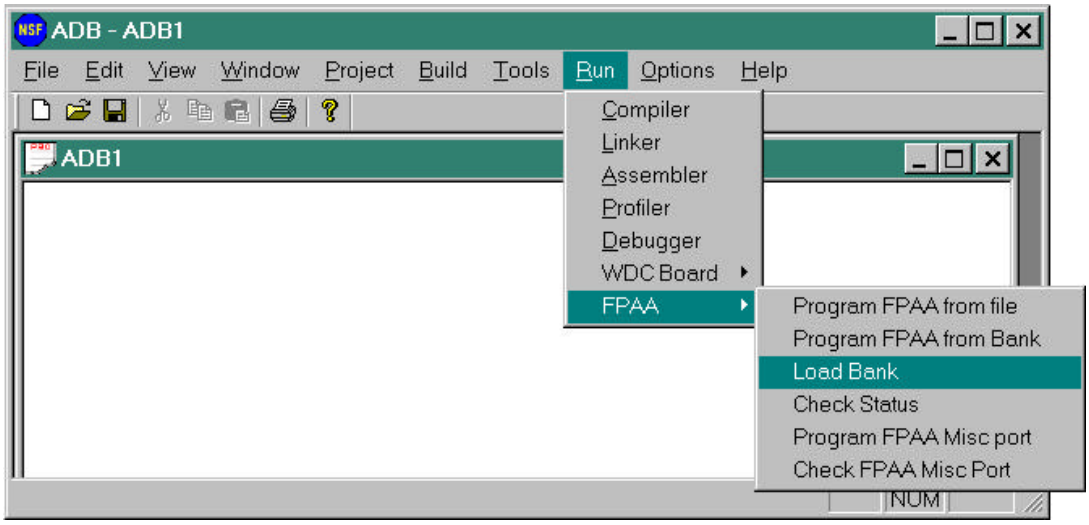

Figure 2. View of the window controlling the ADB operations.

4. Example - FPAA/FPGA application

An example of two FPAA's working in parallel is shown in Fig. 3. The input signal enters to both FPAA circuits. However the output is multiplexed using the analog multiplexer (***MUX).*** Consequently, one FPAA may be used for actual processing of input signal while the other one is on stand-b mode ready to be programmed under the control of digital system. The digital system obtains an external input, which determines about the switching of filter parameters. The physical arrangement of the hardware involving WDC development board, 2 FPAA's, FPGA, PC and monitor is shown in Fig.4.

Optimization of performance includes time for programming of FPAA, determination of time for transients resulting from switching the reprogrammed FPAA on-line, and selection of final moment for multiplexing the output signals. The FPAA programming time depends on method of transfer of bit stream containing the filter circuit structure and parameter values, which are determined by the setting of switched capacitors. The transient time depends on the filter transfer function and its parameters. Research of this matter resulted in some analytical formulations for simple cases and look-up tables for more involved transfer functions. The selection of moment of multiplexing can result in discontinuities of output signal, which generates spurious signals perturbing the filter operation. Several performance metrics may be used to characterize the behavior of the filter. In our investigations to date we used the Spurious Free Dynamic Range (SFDR), which is commonly used to evaluate performance of wireless communication circuits. The research resulted in useful relations determining the optimal multiplexing moment for several filter structures. Some theoretical results were confirmed by experimentation with the hardware under development.

5. Conclusions

The described analog-digital development system is very suitable for research on behavioral modeling of mixed-signal systems and experimental verification of such
It will be also useful in fast prototyping of mixed-signal systems and verification of system concepts. modeling. It is anticipated that its primary application will be in research and academic laboratories, because of its flexibility and low cost.

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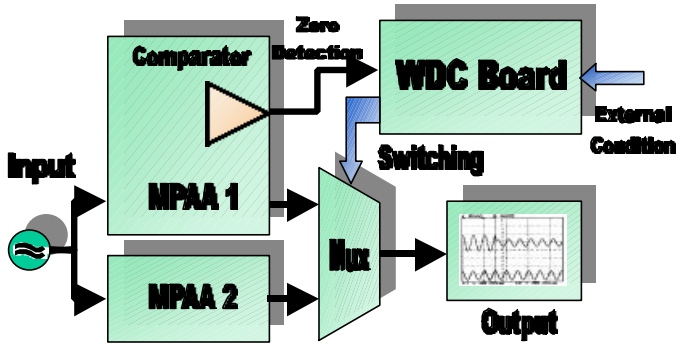

Fig. 3. Schematic of implementation of adaptive filter with use of 2 FPAA's and an analog multiplexer (***MUX***).

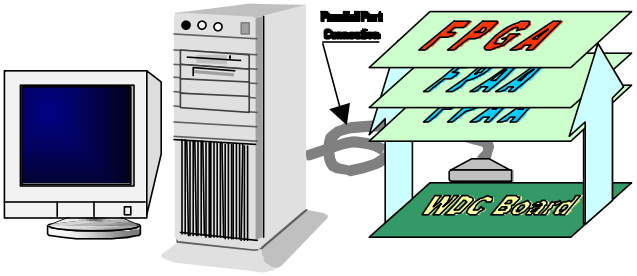

Figure 4. Physical arrangement of FPAA's, FPGA, WDC development board, PC , and monitor for experimental implementation of adaptive filtering.