PNP current mirror

Schematic

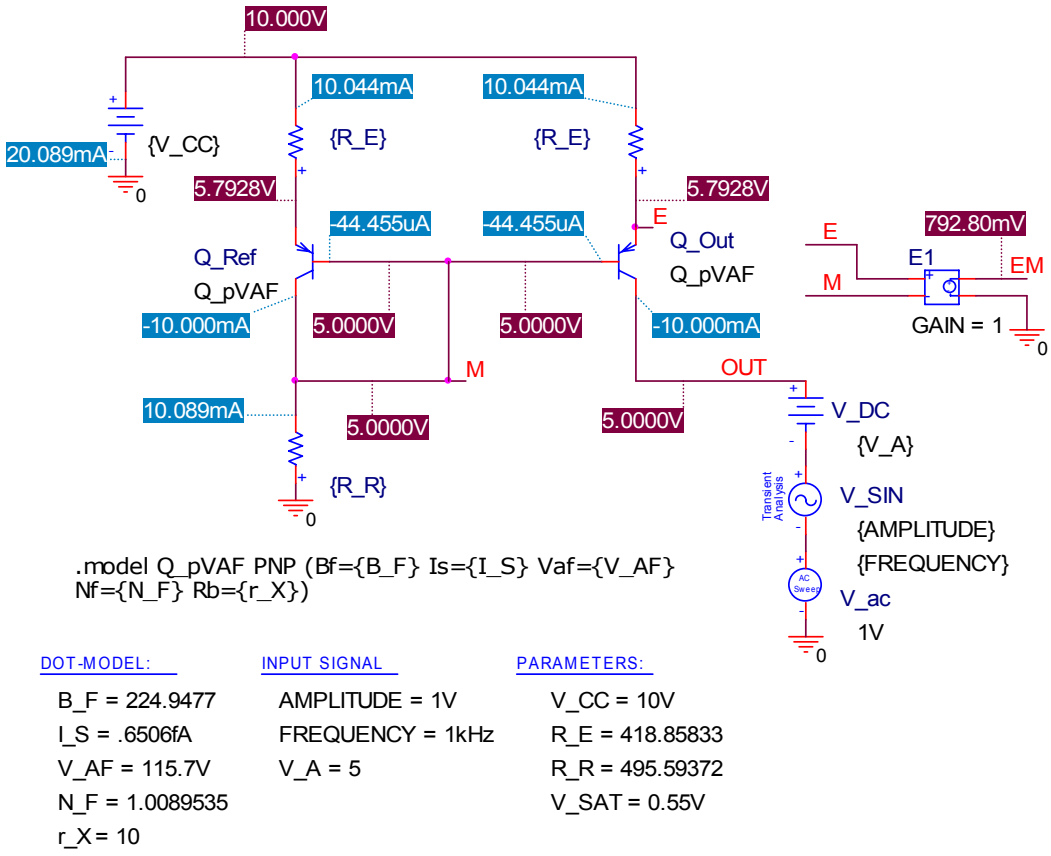

Figure 1
Circuit for pnp current mirror using simple device with dot-model statement shown

Figure 1 shows a schematic for a pnp current mirror.[1] The purpose of the mirror is to emulate an ideal current source, that is, to provide the same DC current through the output node regardless of the voltage applied, DC or transient.

How does it work?

The basic idea behind the circuit is that the left side draws a current through the reference transistor setting up a corresponding emitter-base voltage. Because the circuit is

[1] Also shown in Figure 1 is an evaluator circuit using PSPICE VCVS Part E just to display the value of V_{EM} on the schematic for easy comparison with the spreadsheet constructed in this chapter.

symmetric (assuming the output and reference transistors are alike) the same V_{EB} appears at the output transistor, so the same current flows there (it is *mirrored*), almost independent of the voltage V_A because V_A hardly affects V_{EB}.

Unfortunately, the mirror is not entirely successful, having these limitations:

1. It provides a nearly constant DC current only over a limited range of voltages. This limitation arises at voltages $V_A > V_M$ (V_M = mid-base voltage), where the output transistor Q_{Out} leaves active mode and goes into saturation.
2. Even in the range of voltages $V_A < V_M$ where Q_{Out} is active, the current is not strictly constant, but varies somewhat with V_A. That is, the circuit resembles a Norton source with a finite Norton resistance instead of an ideal current source. This limitation is due to the finite output resistance of transistor Q_{Out}.

The above limitations are illustrated in Figure 2.

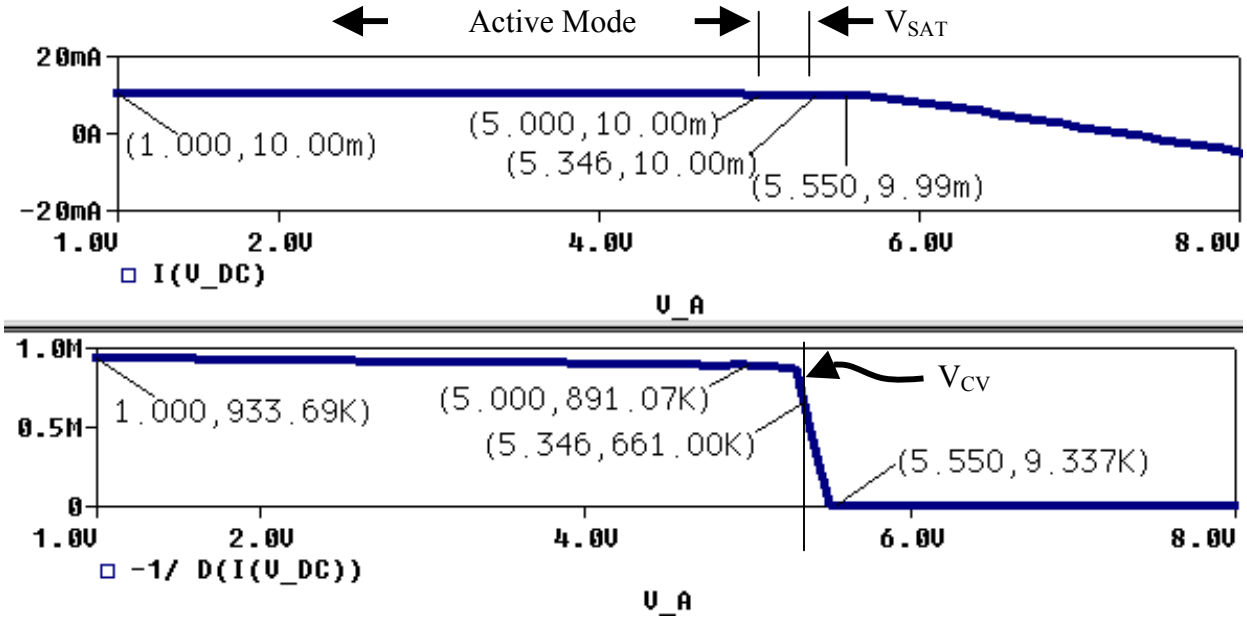

Figure 2

Circuit output behavior for Figure 1; at the compliance voltage V_{CV} where output resistance begins a rapid drop to low values, the output transistor is in saturation by $V_{BC} = -V_{SAT}$

The top panel in Figure 2 shows the current-voltage *I-V* behavior of the mirror. It delivers a DC current of 10 mA for voltages below approximately 5.55V. The lower panel shows the resistance of the mirror, determined as the inverse of the derivative of the current by voltage. It shows that this resistance is high (934 kΩ at V_A = 1 V), but not quite constant, and drops suddenly just above $V_A = V_M$ = 5 V. The drop-off voltage is called the *compliance voltage* V_{CV} of the mirror, and the voltage range where nearly

constant DC current is delivered is the *compliance range* of the mirror. If we choose the bias at 3 dB roll-off of resistance as the verge of the drop, we find the compliance voltage is V_{CV} = 5.346 V from Figure 2. At this bias, the output transistor is in saturation by an amount $V_{BC} = -V_{SAT} = -0.346$ V. At the point where the DC *current* has just begun to drop (V_A = 5.55 V) the output resistance of the mirror already is at a very low value of only 9.34 kΩ, showing that the Norton resistance of the mirror is much more sensitive to saturation of the output transistor than is the DC current itself.

Because the limitations of the mirror depend on the limitations of the transistor, we need a transistor model that includes the Early voltage of the device. Otherwise, the mirror would still have a voltage limitation, but would be an ideal current source as long as Q_{Out} was active. Hence, we have the dot-model statement in Figure 1, discussed in detail shortly.

Design goal

We want to design the circuit of Figure 1 to meet specifications on DC current level I_C at $V_A = V_M$ (both transistors with V_{BC} = 0 V), on compliance voltage V_{CV} (taken as a specification on V_M because V_M is unambiguous and differs from V_{CV} by only the small voltage V_{SAT} discussed later[2]), and specifications on output resistance R_N (Norton resistance) of the mirror. The variables at our disposal are the leg resistor value R_E and the reference resistor value R_R, so unless we are lucky only two of the three specifications can be satisfied, and a trade-off will be necessary. For this purpose we will set up a spreadsheet incorporating the hand analysis below.

AC and DC beta-values

For the dot-model statement of Figure 1, the small-signal AC β-value, which will be called β_{AC}, is the same as the DC β-value, which is called β_{DC}. However, that is not so for more complex models, so we include this difference in the equations here. EQ. 1 defines DC β:

[2] The value of V_{SAT} is expected to be somewhere around 0.5 V, but its value is unknown without a simulation. It varies with the type of transistor and with the current and bias conditions.

EQ. 1

$$\beta_{DC} = \frac{I_C}{I_B},$$

while AC β is defined by:

EQ. 2

$$\beta_{AC} = \frac{dI_C}{dI_B} = \frac{dI_C}{d\left(I_C / \beta_{DC}\right)} = \frac{1}{\frac{1}{\beta_{DC}} - \frac{I_C}{\beta_{DC}^2}\frac{d\beta_{DC}}{dI_C}} = \frac{\beta_{DC}}{1 - \frac{I_C}{\beta_{DC}}\frac{d\beta_{DC}}{dI_C}}.$$

According to EQ. 2, β_{AC} is different from β_{DC} if β_{DC} depends on I_C. For the dot-model statement of Figure 1 β_{DC} does not depend on I_C, but for real transistors it does. So, for real transistors, β_{DC} and β_{AC} are the same only at the maximum in the β_{DC} vs. I_C curve. An example is shown in Figure 3 below.

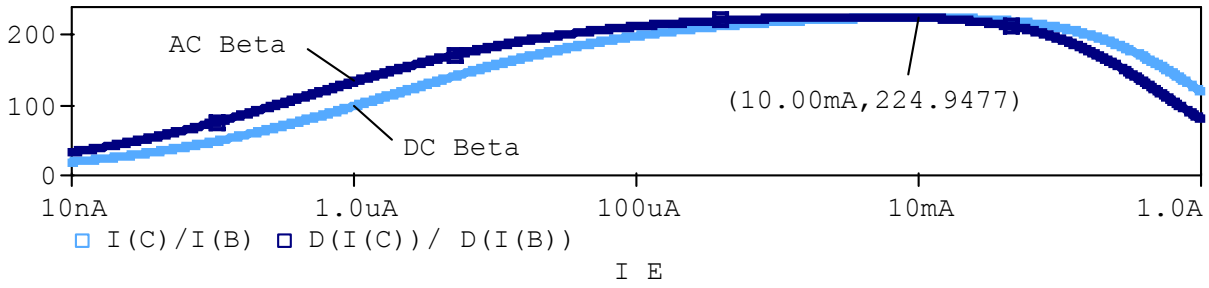

Figure 3

Comparison of AC and DC β-values as a function of emitter current I_E for the Q2N2907A pnp-transistor with V_{BC} = 0 V

Figure 3 shows the current dependence of the two β's for the Q2N2907A transistor using the PSPICE dot model statement for this transistor. It can be seen that the two β's agree at the maximum in β_{DC} near an emitter current of I_E = 10 mA. In addition, $\beta_{AC} > \beta_{DC}$ when β_{DC} has positive derivative, as predicted by EQ. 2.

Figure 3 is generated using the circuit of Figure 4 with a DC SWEEP analysis to sweep I_E. Zero-bias DC voltage sources are inserted in the base and collector leads and named B and C to indicate that the currents I(B) and I(C) going through them are the base and collector currents.

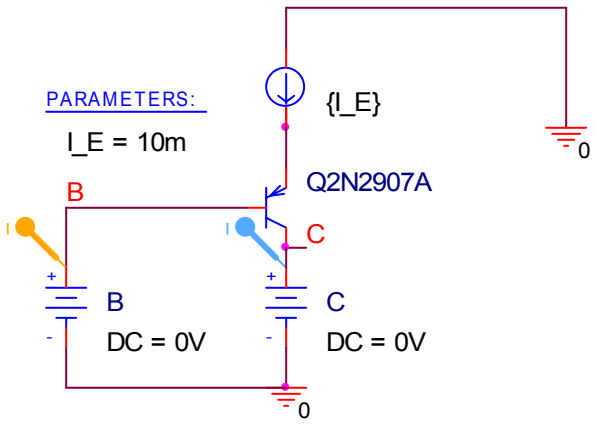

Figure 4
Test circuit for generating AC and DC β-plots of Figure 3

The Q_pVAF dot-model parameters

To allow later comparison with the Q2N2907A, the dot model statement of Figure 1 is introduced, namely

```
.model Q_pVAF PNP (Bf={B_F} Is={I_S} Vaf={V_AF} Nf={N_F} Rb={r_X})
```

which can be compared with the dot-model statement for the Q2N2907A:

```
.model Q2N2907A PNP (Is=650.6E-18 Xti=3 Eg=1.11 Vaf=115.7 Bf=231.7 Ne=1.829
+            Ise=54.81f Ikf=1.079 Xtb=1.5 Br=3.563 Nc=2 Isc=0 Ikr=0 Rc=.715
+            Cjc=14.76p Mjc=.5383 Vjc=.75 Fc=.5 Cje=19.82p Mje=.3357 Vje=.75
+            Tr=111.3n Tf=603.7p Itf=.65 Vtf=5 Xtf=1.7 Rb=10)
*            National pid=63              case=TO18
*            88-09-09 bam      creation
```

provided with PSPICE.

To improve agreement with more realistic dot-model statements like that for the Q2N2907A, the Q_pVAF dot-model statement includes parameters for Early voltage V_{af}, non-ideal diode-law N_f , and internal series base resistance R_b. This dot-model statement corresponds in active mode to the *I-V* relation

EQ. 3

$$I_C = I_S\left[\exp\left(\frac{V_{EBi}}{\eta V_{TH}}\right)-1\right]\cdot\left(1+\frac{V_{BCi}}{V_{AF}}\right),$$

where V_{EBi}, V_{BCi} are the *intrinsic* emitter-base and base-collector voltages, differing from the circuit or *external* values because of the internal base resistance r_X, as discussed shortly. The parameter η is the *ideality factor* or, as referred to in the PSPICE documentation, the *forward current emission coefficient*, also discussed shortly.

Notice the intrinsic emitter-base voltage according to EQ. 3 is given by EQ. 4:

EQ. 4

$$V_{EBi} = \eta V_{TH}\,\ell n\left(1+\frac{I_C}{I_S\left(1+\frac{V_{BCi}}{V_{AF}}\right)}\right)$$

Let's take a closer look at the effects of these parameters.

Early voltage: parameter V_{AF}

The Early voltage enters the current *I-V* relation as shown in EQ. 3. Somewhat less obvious is the Early voltage influence on the transistor β's. The DC base current of the transistor, I_B, does not depend upon the base-collector voltage, so EQ. 5 gives the DC β:

EQ. 5

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{I_C(V_{BC}=0)\left(1+\frac{V_{BC}}{V_{AF}}\right)}{I_B} = \beta_{DC}(V_{BC}=0)\left(1+\frac{V_{BC}}{V_{AF}}\right).$$

That is, the DC β increases with V_{BC} because of the Early effect. The AC β does the same thing if the current dependence of β_{DC} is contained in $\beta_{DC}(V_{BC}=0)$. That is,

EQ. 6

$$\beta_{AC} == \beta_{AC}(V_{BC}=0)\left(1+\frac{V_{BC}}{V_{AF}}\right).$$

Base resistance: parameter R_b and the intrinsic base resistance r_X

The introduction of the base resistance r_X introduces some complications into our equations because the device behavior is governed by the *internal* V_{EBi} of the transistor, which differs from the *external* V_{EB} of the circuit by the voltage drop across r_X. See Figure 5.

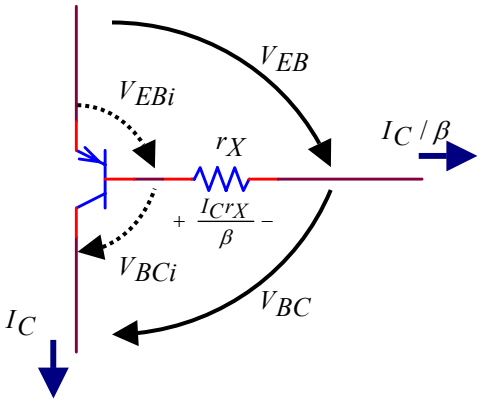

Figure 5
Internal and external voltages related to r_X: $V_{EBi} < V_{EB}$ because of drop across r_X, while $V_{BCi} > V_{BC}$

According to Figure 5, the internal and external emitter-base voltages are related as:

EQ. 7

$$V_{EBi} = V_{EB} - \frac{I_C}{\beta_{DC}} r_X .$$

Combining EQ. 7 with EQ. 4 we find V_{EB} is related to the current by

EQ. 8

$$V_{EB} = \eta V_{TH} \ell n \left(1 + \frac{I_C}{I_S \left(1 + \frac{V_{BCi}}{V_{AF}} \right)} \right) + \frac{I_C}{\beta_{DC}} r_X .$$

In addition to its effect on V_{EBi}, the voltage drop across r_X causes a non-zero *internal* V_{BCi} of the transistor, even though the external circuit $V_{BC} = 0$ V. (Consider Figure 5 for the case where $V_{BC} = 0$ V.)

A non-zero V_{BCi} means the Early effect comes into play, affecting the current and the beta values of the transistor, so the transistor betas increase according to

EQ. 9

$$\beta(V_{BCi}) = \beta(V_{BC} = 0V) \left(1 + \frac{V_{BCi}}{V_{AF}} \right).$$

The value of V_{BCi} is given by Ohm's law as EQ. 10:

EQ. 10

$$V_{BCi} = \frac{I_C}{\beta(V_{BCi})} r_X .$$

Solving the quadratic found by substituting EQ. 9 into EQ. 10, we find V_{BCi} as shown in EQ. 11 next:

EQ. 11

$$V_{BCi} = \frac{V_{AF}}{2} \left[\left(1 + \frac{4 I_C r_X}{\beta(V_{BC} = 0)\, V_{AF}} \right)^{1/2} - 1 \right].$$

Parameter r_X is set using dot-model parameter R_b, namely, $r_X = R_b$.

Current dependence of small-signal parameters; parameter η

You may recall the current and voltage dependence of the transistor small-signal parameters for a simple bipolar exhibiting Early effect. In particular,

EQ. 12

$$r_O = \frac{V_{AF}}{I_C(V_{BC} = 0)} = \frac{V_{AF} + V_{BC}}{I_C(V_{BC})}, \quad r_\pi = \frac{\beta_{AC}}{g_m} \approx \frac{\beta_{AC} V_{TH}}{I_C} .$$

In EQ. 12, r_O = output resistance, r_π = base input resistance, g_m = small-signal transconductance, V_{AF} = Early voltage and V_{TH} = thermal voltage ($k_BT/q \approx 25.864$ mV @ 27° C). EQ. 12 for r_O does not agree with most textbooks, but it does agree with PSPICE and transistor physics.

In real transistors the ideal diode law is not satisfied. To help match this reality, the Q_pVAF dot-model statement includes parameter N_f. When this parameter is used, the transconductance and base resistance are given by the relations:

EQ. 13

$$g_m = \frac{1}{\eta}\frac{I_C}{V_{TH}}, \quad r_\pi = \frac{\beta_{AC}}{g_m} = \eta\frac{\beta_{AC}V_{TH}}{I_C},$$

where parameter η is the before-mentioned ideality factor also known as the forward current emission coefficient.

Parameter η is specified by dot-model parameter N_f, namely $\eta = N_f$.

Setting η

How can η be found? Let's assume we want the value of η that makes our Q_pVAF-model fit the Q2N2907A. The same approach works for other models. Figure 5 puts the Q2N2907A and Q_pVAF in identical circuits. These circuits set the external V_{BC} = 0 V, which is the case for the mirror at the design point. Then we find the *external* g_m-values by running a DC sweep of I_E and taking derivatives, as shown in Figure 7. We set the N_f value to make the two g_m-values the same at the current level of interest, namely 10 mA in this case. We set

EQ. 14

$$N_f = \frac{g_m(Q2N2907A)}{g_m(Q\_pVAF)} = 0.3784089/0.3750509 = 1.0089535.$$

The *external* g_m-values are related to the *internal* g_m-values by EQ. 15 (using EQ. 7 for V_{EBi}):

EQ. 15

$$g_m(ext) = \frac{\partial I_C}{\partial V_{EB}} = \frac{\partial I_C}{\partial V_{EBi}}\frac{\partial V_{EBi}}{\partial V_{EB}} = g_{mi}\left(1 - \frac{r_X}{\beta_{DC}}g_{mi}\right),$$

where the internal transconductance $g_{mi} = \partial I_C/\partial V_{EBi}$. EQ. 15 is interesting mainly because it shows setting the external g_m-values equal also makes the internal g_m-values equal.[3, 4]

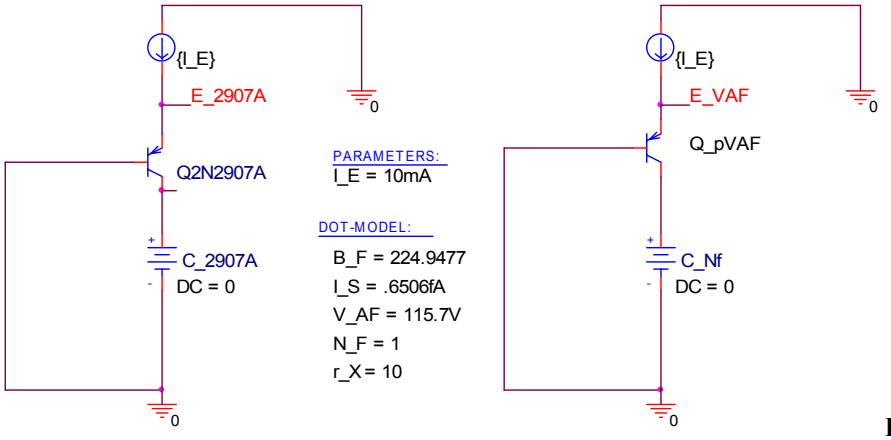

Figure 6

Test circuit for finding value of dot-model parameter N_f; notice that $N_f = 1$ in this test

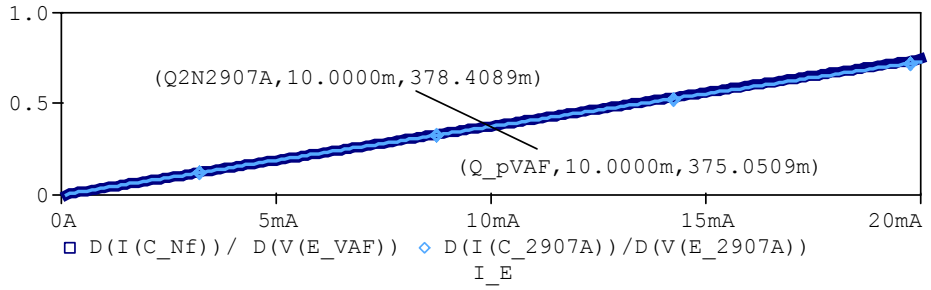

Figure 7

Comparison of external g_m values when $N_f = 1$; we want to increase N_f to make these two values the same

Finding N_f this way makes the simple transistor model Q_pVAF resemble closely the more realistic model Q2N2907A, and in particular makes sure that the small-signal parameters g_m and r_π at the design point are the same.

Hand analysis

Q-point analysis

The design is done for the case $V_A = V_M$ because that makes analysis simpler. If instead we choose $V_A < V_M$, the two transistors have different V_{BC} values and that affects the currents and β-values because of the Early effect. For $V_A = V_M$, applying KVL to the output side of the circuit of Figure 1, we find a relation for R_E given by EQ. 16 below:

EQ. 16

[3] Technically there are two values for g_{mi} for each g_m, and we want the value very close to g_m.

[4] It is the *internal* g_m-value that is given by EQ. 13 and is listed in the PROBE output file.

$$R_E = \frac{V_{CC} - V_{EB} - V_M}{I_C\left(1 + 1/\beta_{DC}\right)}.$$

In EQ. 16 the various symbols are: I_C = output (collector) current of Q_{Out}, V_{EB} = emitter-base voltage of Q_{Out}, V_M = base voltage of both transistors, β_{DC} = DC beta of Q_{Out}. Applying KVL to the left side of the mirror we find R_R is given by[5]

EQ. 17

$$R_R = \frac{V_M}{I_C\left(1 + 2/\beta_{DC}\right)}.$$

Small-signal analysis

Next we ask just how much the current varies for voltages below the base voltage. That is, what is the slope of the *I-V* curve for $V_A < V_M$. The easiest way to find out is to bias the mirror at some value of V_A below V_M and superpose a small-signal AC voltage V_{ac}. Then the small-signal current I_{ac} that flows is

EQ. 18

$$I_{ac} = \frac{\partial I_C}{\partial V_A} V_{ac} \equiv \frac{1}{R_N} V_{ac},$$

where R_N is the Norton resistance of the mirror, and indicates the rate of variation of the current with applied voltage. The small-signal circuit corresponding to this approach is shown in Figure 8 below.[6] Test current I_x is applied and $R_N = V_x/I_x$.

In Figure 8 the parasitic base resistance r_X is included to allow a closer comparison with the Q2N2907A later on. This resistance is included in Figure 1 by specifying the dot-model parameter R_b, set in the dot-model PARAMETER box to $R_b = r_X$.

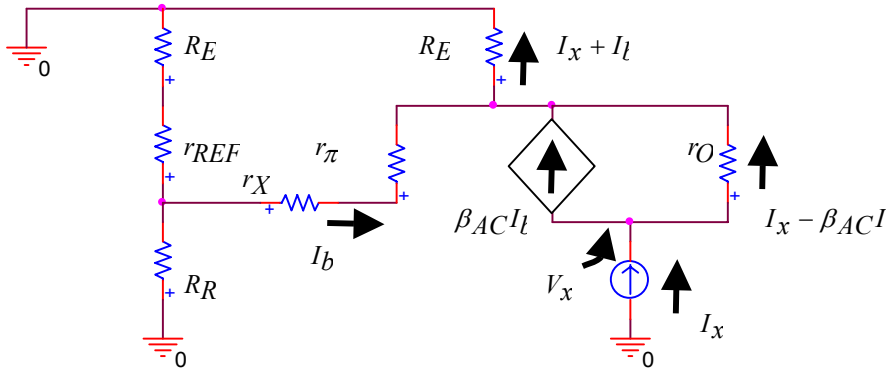

Figure 8

[5] Use KCL at the base of Q_{Out} to derive the factor $(1+2/\beta_{DC})$.

[6] The replacement of transistor Q_{Ref} by the resistor r_{REF} is explained in the Appendix.

Small-signal circuit corresponding to Figure 1

An easy way to solve circuits like this is to determine all the currents and then use KVL. Taking KVL on the left side of the circuit noting that (r_{REF} + R_E) is in parallel with R_R and following I_b through r_π and R_E we find EQ. 19:

EQ. 19

$$I_b[(r_{REF} + R_E)// R_R + r_\pi + r_X] + (I_x + I_b)R_E = 0\,,$$

which determines I_b in terms of I_x as

EQ. 20

$$I_b = -I_x \frac{R_E}{R_E + r_\pi + r_X + (r_{REF} + R_E)// R_R}\,.$$

Then KVL through the right side of the circuit provides

EQ. 21

$$V_x = (I_x - \beta_{AC} I_b) r_O + (I_x + I_b) R_E\,,$$

Collecting terms in I_x and I_b and substituting for I_b from EQ. 20 we find R_N as EQ. 22 next:

EQ. 22

$$R_N = \frac{V_x}{I_x} = r_O \left(1 + \beta_{AC} \frac{R_E}{R_E + r_\pi + r_X + (r_{REF} + R_E)// R_R}\right) + R_E \frac{(r_{REF} + R_E)// R_R + r_\pi}{R_E + r_\pi + r_X + (r_{REF} + R_E)// R_R}$$

.

Notice that for large R_E, the leading term in R_N approaches (β_{AC}+1) r_O, while for small R_E it approaches r_O. So R_N is a large resistance, and increases with R_E. The most ideal current source from the viewpoint of voltage-independent current occurs at large R_E. Resistance R_N has a complex dependence on the specifications for current value and compliance voltage, and an easy way to see the connections is through graphs generated using a spreadsheet. (For example, see Figure 19 and Figure 21 later on.)

Transient analysis

When a large-signal sinusoidal AC voltage of amplitude V_{ac} is applied to the mirror output with DC voltage V_A applied, the instantaneous applied voltage is

EQ. 23

$$\upsilon_A(t) = V_A + V_{ac} \sin(2\pi f t)\,.$$

To avoid driving the output transistor into saturation, where its low resistance will cause a large AC current spike, the DC bias must be chosen *below* the compliance voltage V_{CV} by at least the AC signal amplitude V_{ac}, that is, we require

EQ. 24

$$V_A \le V_{CV} - V_{ac}\,.$$

Spreadsheet

The hand analysis is put into the spreadsheet as shown in Figure 9. The diode-connected reference transistor resistance is denoted by r_REF, following the analysis in the appendix. To avoid round-off error, a series expansion is used for V_BCi at small values (an IF STATEMENT represents $\sqrt{(1+x)}-1$ by a series for arguments $x < 2 \times 10^{-5}$).[7] The numerical values corresponding to Figure 9 are shown in Figure 10.

In Figure 10 the values for the transistor parameters are selected to represent the QN2907A pnp bipolar transistor parameters included with PSPICE. The values for β_{DC0} and β_{AC0} are determined as shown in Figure 3 for the specified current level of $I_C = 10$ mA at $V_{BC} = 0$V.

The Norton resistance is found using the AC beta from EQ. 9 and the small-signal circuit of Figure 8.

pnp Mirror Design			
Input	pi	pi	3.1415926
	Thermal voltage	V_TH	0.025864
	Supply voltage	V_CC	10
	Early voltage	V_AF	115.7
	DC Beta (VBC=0)	B_DC0	224.9477
	AC Beta (VBC=0)	B_AC0	224.9477
	Scale current	I_S	0.0000000000000006506
	Forward emission coeff	N_F	1.0089535
Specifications	Mid-base voltage	V_M	5
	DC current (mA)	I_C_mA	10
Calculated	DC Current (A)	I_C	=I_C_mA/1000
	4*I_C*r_X/(B_DC0*V_AF)	x	=4*I_C*r_X/(B_DC0*V_AF)
	Series for √(1+x)-1	Series	=0.5*x-0.5*0.5*x^2/2+0.5*0.5*1.5*x^3/6
	Intrinsic VBC	V_BCi	=IF(x<0.00002,(V_AF/2)*Series,(V_AF/2)*(SQRT(1+x)-1))
	Intrinsic VEB	V_EBi	=N_F*V_TH*LN(I_C/((1+V_BCi/V_AF)*I_S))
	BetaDC with V_BC	B_DC	=B_DC0*(1+V_BCi/V_AF)
	Extrinsic VEB	V_EB	=V_EBi+I_C*r_X/B_DC
	Leg R	R_E	=(V_CC-V_EB-V_M)/(I_C*(1+1/B_DC))
	Reference R	R_R	=V_M/(I_C*(1+2/B_DC))
Small Signal	Parasitic base R	r_X	10
	Beta with V_BC	B_AC	=B_AC0*(1+V_BCi/V_AF)
	transconductance	g_m	=I_C/(N_F*V_TH)
	base R	r_PI	=B_AC/g_m
	output R	r_O	=(V_AF+V_BCi)/I_C
	diode R	r_REF	=N_F*V_TH/I_C/(1+(1/B_AC)/(1+r_X/r_PI))
	(rREF+RE)//RR	R_EFF	=1/(1/R_R+1/(r_REF+R_E))
	Denominator	Den	=R_E+r_PI+r_X+R_EFF
	Norton R	R_N	=r_O*(1+B_AC*R_E/Den)+R_E*(R_EFF+r_PI+r_X)/Den

Figure 9
Input worksheet for current mirror design project

[7] Syntax of the IF STATEMENT is described in Chapter 3, or in EXCEL help. Click on HELP and type "if function" in the SEARCH BOX.

pnp Mirror Design			
Input	pi	pi	3.1415926
	Thermal voltage	V_TH	0.025864
	Supply voltage	V_CC	10
	Early voltage	V_AF	115.7
	DC Beta (VBC=0)	B_DC0	224.9477
	AC Beta (VBC=0)	B_AC0	224.9477
	Scale current	I_S	6.506E-16
	Forward emission coeff	N_F	1.0089535
Specifications	Mid-base voltage	V_M	5
	DC current (mA)	I_C_mA	10
Calculated	DC Current (A)	I_C	0.01
	4*I_C*r_X/(B_DC0*V_AF)	x	1.5369E-05
	Series for √(1+x)-1	Series	7.68446E-06
	Intrinsic VBC	V_BCi	4.4454607E-04
	Intrinsic VEB	V_EBi	0.79235197
	BetaDC with V_BC	B_DC	224.9485643
	Extrinsic VEB	V_EB	0.792796512
	Leg R	R_E	418.85833
	Reference R	R_R	495.59372
Small Signal	Parasitic base R	r_X	10
	Beta with V_BC	B_AC	224.9485643
	transconductance	g_m	0.38320676
	base R	r_PI	587.01618
	output R	r_O	11570.04445
	diode R	r_REF	2.5982006
	(rREF+RE)//RR	R_EFF	227.76419
	Denominator	Den	1243.6387
	Norton R	R_N	8.8842708E+05

Figure 10
Numerical values for the design in Figure 1

Verification of spreadsheet

Q-point verification

When the spreadsheet values for R_E and R_R are pasted into PSPICE, the Q-point results are seen in Figure 1. They agree with the specifications of I_C = 10 mA and V_M = 5 V. In addition, we can look at the small-signal results. The PROBE output file is shown in Figure 11 below. Parameters r_O, r_π and g_m agree with the spreadsheet.

NAME	Q_Q_Out	Q_Q_Ref
MODEL	Q_pVAF	Q_pVAF
IB	-4.45E-05	-4.45E-05
IC	-1.00E-02	-1.00E-02
VBE	-0.793	-0.793
VBC	-3.05E-06	0
VCE	-0.793	-0.793
BETADC	225	225
GM	0.383	0.383
RPI	587	587
RX	10	10
RO	1.16E+04	1.16E+04
CBE	0.00E+00	0.00E+00
CBC	0.00E+00	0.00E+00
CJS	0.00E+00	0.00E+00
BETAAC	225	225
CBX/CBX2	0.00E+00	0.00E+00
FT/FT2	6.10E+18	6.10E+18

Figure 11
PROBE output file for case of Figure 1; V_{BC} of Q_{Out} is not quite zero, indicating some inaccuracy

Small-signal verification

The Norton resistance is checked using a small-signal AC SWEEP analysis, as shown in Figure 12. The discrepancy with the spreadsheet is about 2/100 %.

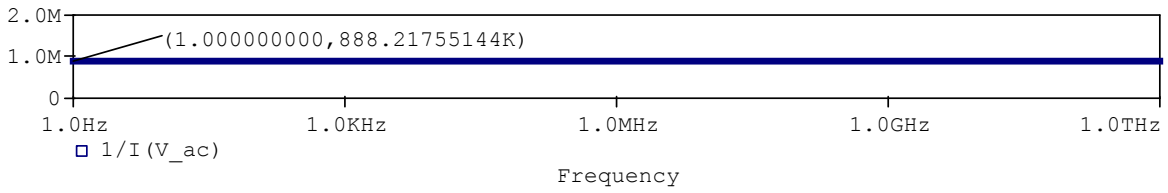

Figure 12
Determination of Norton resistance using small-signal AC SWEEP with a 1 V AC input signal

To check that the discrepancy between PSPICE and the spreadsheet is not some algebraic problem in our small-signal analysis, we can check the analysis of Figure 8 using PSPICE. We set up the PSPICE circuit shown in Figure 13 below:

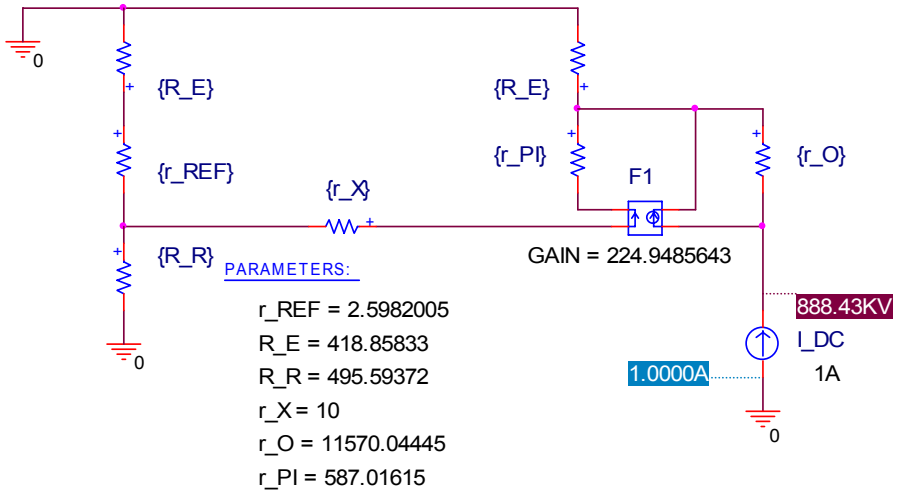

Figure 13
Small-signal circuit corresponding to Figure 8 to check analysis for Norton resistance R_N

The circuit of Figure 13 contains no capacitances so a DC analysis is sufficient. The circuit is linear, so the ratio of the voltage across the test source to the current in the test source does not depend on the value of the current, which we take as 1 A to make calculation easy. Then the resistance looking into the circuit is equal numerically to the voltage at the input.

Running the BIAS POINT analysis the results shown in Figure 13 indicate the Norton resistance is R_N = 888.43 kΩ, compared to 888.43 kΩ from the spreadsheet. Therefore, the analysis of the circuit is accurate and the discrepancy in Figure 12 comes from another source. It does not appear large enough to have practical importance.

Transient behavior

The spreadsheet has not been extended to treat behavior where the output transistor is saturated. However, we can make transient analyses to compare with the behavior seen in Figure 2, providing a check on the concepts behind the mirror design. We set up the DC bias using the parameter V_SAT, as shown in Figure 14. When V_SAT = 0V, the DC bias is set below V_B by the AC amplitude, so EQ. 24 is satisfied and the output transistor always is active. As V_SAT is increased, the output transistor goes further and further into saturation, and the mirror resistance falls rapidly.

DOT-MODEL:	INPUT SIGNAL	PARAMETERS:
B_F = 224.9477	AMPLITUDE = 1V	V_CC = 10V
I_S = .6506fA	FREQUENCY = 1kHz	R_E = 418.85833
V_AF = 115.7V	V_A = {5-AMPLITUDE+V_SAT}	R_R = 495.59372
N_F = 1.0089535		V_SAT = 0.346V
r_X = 10		

Figure 14
Introduction of V_SAT to describe how far into saturation the output transistor is driven at the top of the AC signal

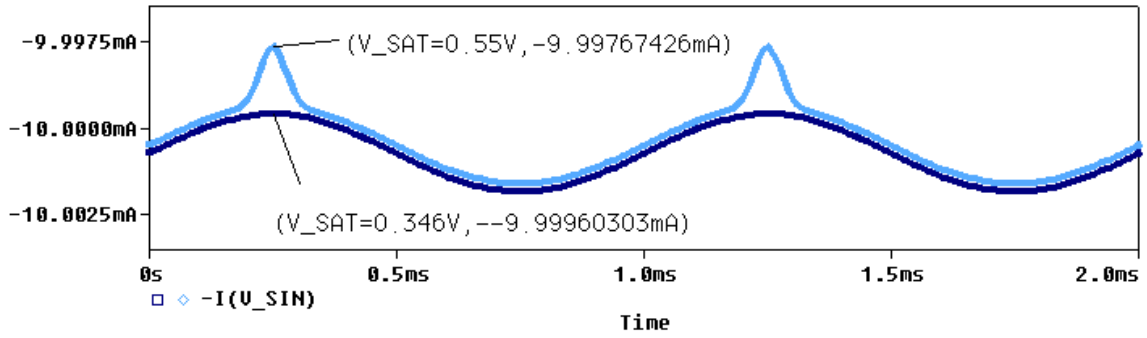

Figure 15
Output current for various values of V_SAT

Figure 15 shows that only slight peaking of output current occurs at V_SAT = 0.346V, the point in Figure 2 where the mirror resistance begins to drop, but becomes evident as V_SAT is increased to 0.55 V, the point in Figure 2 where the mirror resistance has dropped substantially. For larger V_SAT, the peak increases very rapidly. Detection of this peak in AC current is one way to determine the compliance voltage of the mirror.

Comparison with a more realistic transistor model

We replace the simple model of Figure 1 with one of the transistor models provided with PSPICE, namely the Q2N2907A, as shown in Figure 16.[8] The Q-point agrees fairly closely with the spreadsheet because the dot-model parameters in Figure 1 were chosen to agree with this transistor. However, the value of $V_{EB} = V_{EM}$ is not the same as with the simpler model Q_pVAF, V_{EM} = 786 mV compared to 793 mV in Figure 1. The model Q2N2907A is much more complex than the model Q_pVAF, and parameter η only approximates its behavior. An investigation of just what leads to the discrepancy could be a big job. It won't be done here.

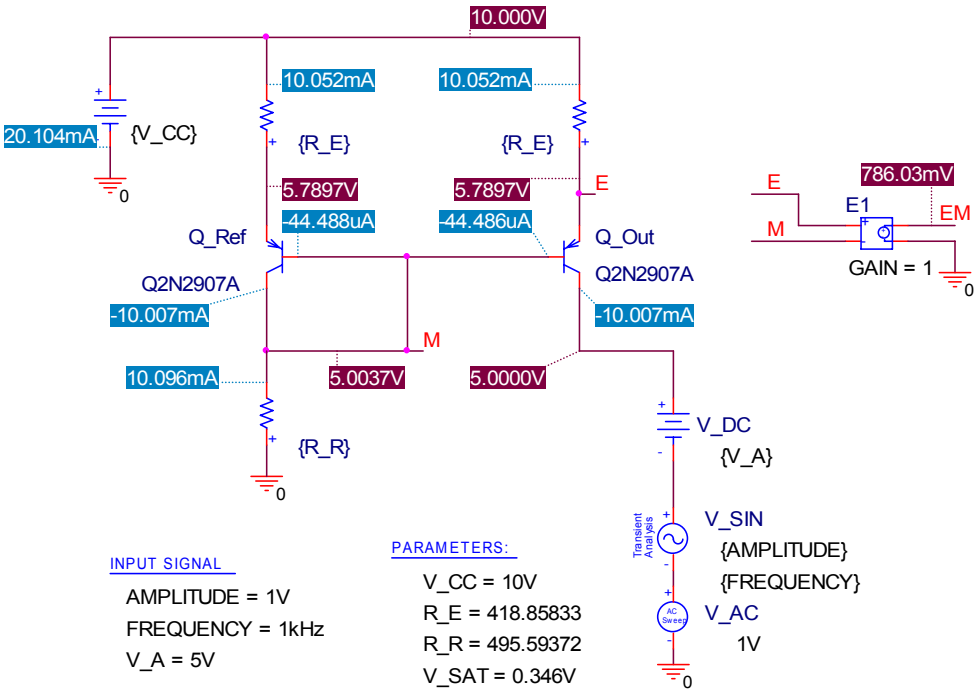

Figure 16
The pnp mirror with the dot-model statement for the Q2N2907A provided with PSPICE

The PROBE output file is shown in Figure 17 below. Comparison with Figure 11 shows the small-signal parameters of the simple model agree, as we intended when setting η.

[8] The Q2N2907A is pasted on the schematic by selecting the schematic, opening menu PLACE/PART and typing Q2N2907A into the PART window. The EVAL library must be enabled.

NAME	Q_Q_Out	Q_Q_Ref
MODEL	Q2N2907A	Q2N2907A
IB	-4.45E-05	-4.45E-05
IC	-1.00E-02	-1.00E-02
VBE	-0.786	-0.786
VBC	0.00367	0
VCE	-0.79	-0.786
BETADC	225	225
GM	0.383	0.383
RPI	587	587
RX	10	10
RO	1.16E+04	1.16E+04
CBE	2.66E-10	2.66E-10
CBC	1.48E-11	1.48E-11
CJS	0.00E+00	0.00E+00
BETAAC	225	225
CBX/CBX2	0.00E+00	0.00E+00
FT/FT2	2.17E+08	2.17E+08

Figure 17

PROBE output file for the mirror using Q2N2907A transistors

The small-signal Norton resistance is found in Figure 18. Unlike Figure 12, Figure 18 shows frequency roll-off due to the parasitic capacitances of the Q2N2907A. The ideal transistor model Q_pVAF in Figure 1 doesn't include any capacitances.

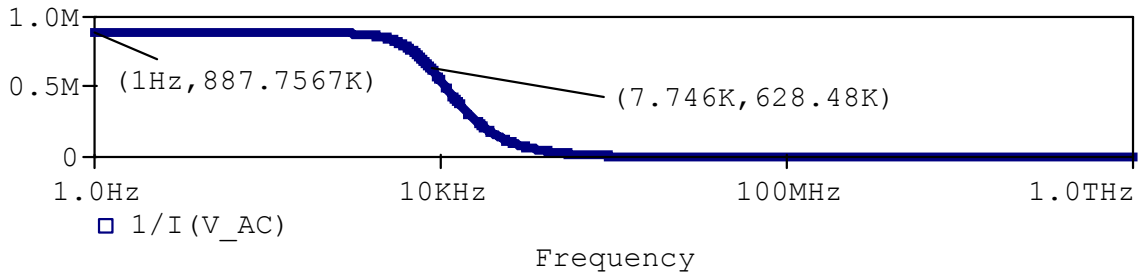

Figure 18

AC Norton resistance vs. frequency for Figure 16

The value R_N = 887.8 kΩ in Figure 18 is close to the spreadsheet prediction of R_N = 888.4 kΩ.

Using the spreadsheet as a design tool

The example of Figure 1 satisfies a specification of 10 mA output current for voltages below V_A = 5 V. However, other specifications involving the output resistance of the mirror could arise. To see what compromises are necessary, trade-off charts are easily set up as shown in Figure 19 below.

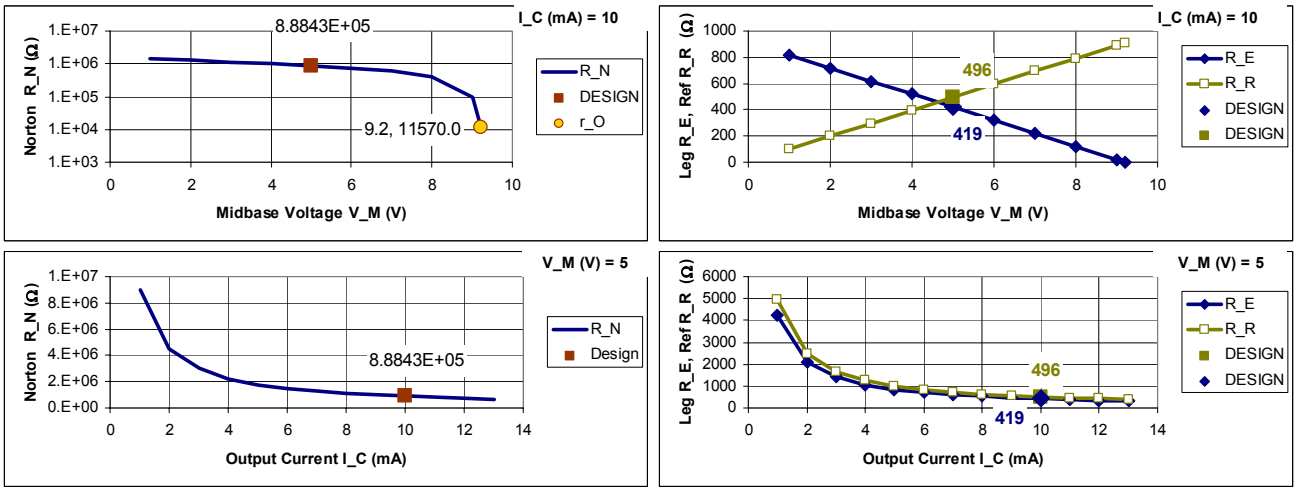

Figure 19
Trade-off charts based on the spreadsheet of Figure 9

As usual, we first try to understand the trends shown in the charts to gain some understanding of the circuit behavior. Let's begin by thinking about the downward trends in R_N as either the mid-base voltage V_M increases or the output current increases.

Trend of R_N with mid-base voltage V_M when I_C = constant

For V_M to increase, the voltage drop across R_E must be reduced because V_M is mainly determined by V_{CC} and the drop across R_E. At a fixed output current the only way to reduce this drop is by reduction of R_E. EQ. 22 shows that reduction of R_E reduces R_N because the contribution to R_N from the term

$$r_O \beta_{AC} \frac{R_E}{R_E + r_\pi + r_X + (r_{REF} + R_E) /\!/ R_R}$$

drops as R_E goes down. For $R_E = 0\ \Omega$, $R_N = r_O$, which is as low as it gets.

Trend of R_N with output current I_C when V_M = constant

For I_C to increase, the current on the left side of the mirror must increase. One way this can happen is to reduce R_R, because the current basically is determined by V_M/R_R. However, such an increase in current will naturally tend to increase the drop across R_E, which cannot happen if V_M is maintained. Therefore, R_E must drop as I_C increases, and as already observed, this causes R_N to drop.

Trend of R_R and R_E with V_M when I_C = constant

It already is argued that R_E drops as V_M increases. Also, as V_M increases the current tends to increase because it is controlled by V_M/R_R. However, an increase in current is not allowed if I_C is held fixed, so R_R must increase to maintain the current. Thus, R_R and R_E have opposite trends, as shown in the upper right panel of Figure 19.

Trend of R_R and R_E with I_C when V_M = constant

From the above arguments R_R and R_E both must drop as I_C increases to maintain V_M.

This discussion clarifies how R_R and R_E affect the mirror properties.

Example design

As a different design problem, let's consider a case where we want to specify V_M and R_N but don't care much about the current I_C, except it should be as large as possible. To be specific, let's request that $V_M = 2$ V and $R_N \geq 1$ MΩ for $V_A \leq V_M = 2$ V. We require the amplifier be built with Q2N2907 transistors.

Answer: The design is found using GOAL SEEK. We set $V_M = 2$ V in the input worksheet, and ask GOAL SEEK to set the output resistance at $R_N = 1$ MΩ by varying I_C_mA. See Figure 20.

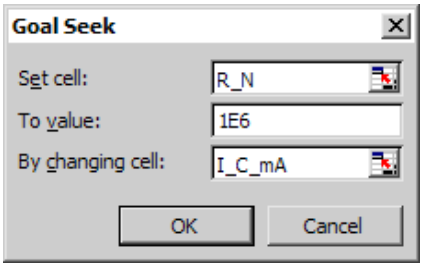

Figure 20
Using GOAL SEEK to find correct I_C for $R_N = 1$ MΩ

The resulting design curves are shown in Figure 21.

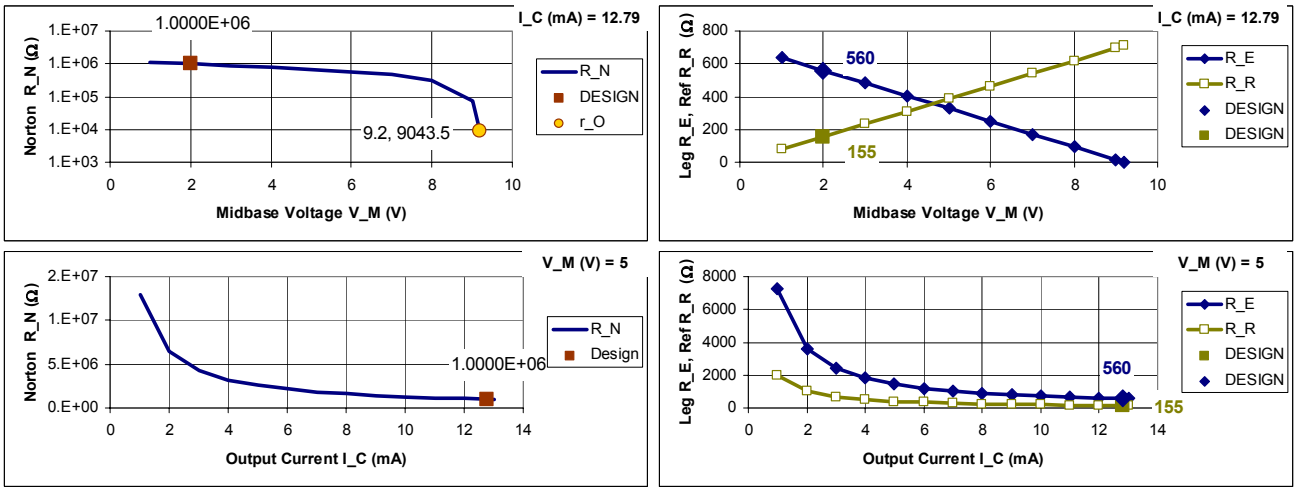

Figure 21

Design curves with design point for the requested specs of $V_M = 2$ V and $R_M = 1$ MΩ

The spreadsheet suggests $R_E = 560$ Ω and $R_R = 155$ Ω, and that the output current will be $I_C = 12.8$ mA. This current is larger than the $I_C = 10$ mA used to calibrate our Q_pVAF model parameters, so our values for β's and η may be off a bit, requiring some recalibration. We check out the design using PSPICE.

NAME	Q_Q_Out	Q_Q_Ref
MODEL	Q2N2907A	Q2N2907A
IB	-5.69E-05	-5.69E-05
IC	-1.28E-02	-1.28E-02
VBE	-0.793	-0.793
VBC	0.00147	0
VCE	-0.794	-0.793
BETADC	225	225
GM	0.489	0.489
RPI	458	458
RX	10	10
RO	9.04E+03	9.04E+03
CBE	3.30E-10	3.30E-10
CBC	1.48E-11	1.49E-11
CJS	0.00E+00	0.00E+00
BETAAC	224	224
CBX/CBX2	0.00E+00	0.00E+00
FT/FT2	2.26E+08	2.26E+08

Figure 22

PROBE output file for design

Figure 22 shows the PROBE output file. At this current level β_{DC} and β_{AC} still are close to the values used before. The value of $r_\pi = 458$ Ω compares with a spreadsheet value of $r_\pi = 459$ Ω, so the design shouldn't be too far off.

Figure 23 shows the Q-point at the design condition $V_A = 2$ V $= V_M$. Indeed V_M is very close to the designed-for $V_M = 2$ V.

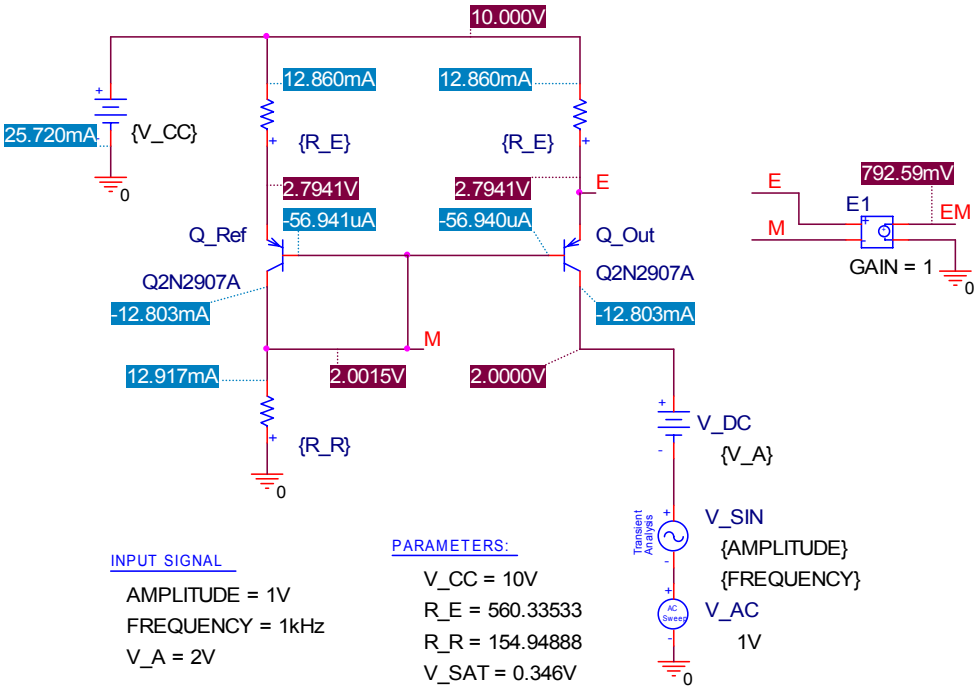

Figure 23

Q-point check on design when $V_A = V_M$ = specified $V_M = 2$ V

Finally, the real comparison of mirror characteristics is shown in Figure 24.

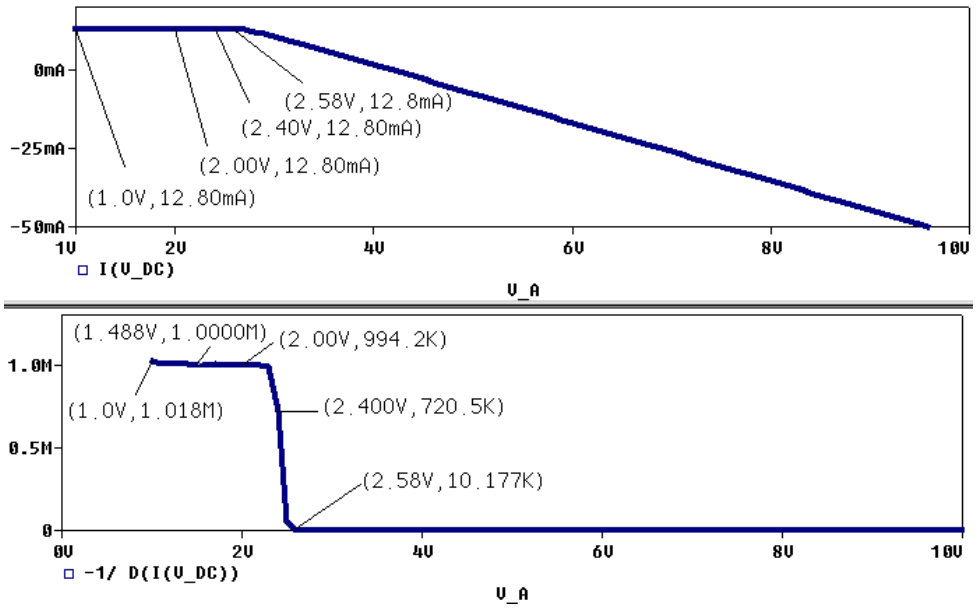

Figure 24

Mirror properties for example design

Figure 24 shows the mirror $R_N > 1$ MΩ for $V_A \leq 1.5$ V, while the spec calls for more room with $R_N > 1$ MΩ for $V_A \leq 2$ V. We have a couple of choices to improve the design. The first is simply to use the trade-off curves to pick better values for R_E and R_R. The second is to recalibrate the model to see if that makes the spreadsheet design

adequate. Because the calibration doesn't seem too far off, the first choice looks more promising. What has to be done to bring the design within specs?

The problem with the design is that V_M is too small. So we could try the spreadsheet again with a larger V_M. That tends to lower the R_N, so I_C has to be adjusted. Iteration is needed, so we set $V_M = 2.5$ V and use GOAL SEEK to find the design with $R_N = 1$ MΩ. For this design the resistance plot is shown in Figure 25. The spreadsheet values are $R_E = 550$ Ω and $R_R = 204.5$ Ω with $I_C = 12.12$ mA. This design meets the spec with $R_N \geq 1$ MΩ for $V_A < 2.3$ V, but we are forced to a lower current.

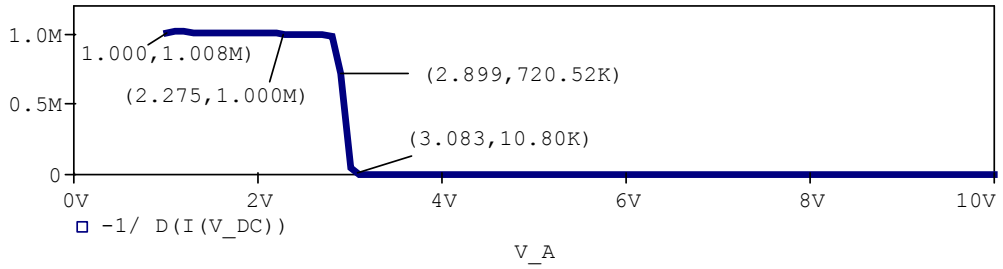

Figure 25
Mirror resistance for iterated design

Comments

The current mirror, a circuit element ubiquitous in analog design, differs from an ideal current source strictly because of the limitations of the bipolar transistors used to build it. For that reason, a somewhat complex model for the transistor is needed to capture the mirror behavior. Nonetheless, a simple spreadsheet is useful to design a current mirror to meet specifications on current level, compliance voltage range and output Norton resistance.

The spreadsheet enables easy exploration of design trade-offs. For example, the designs presented indicate a trend to lower currents as compliance range is increased at a fixed Norton resistance. Qualitative design decisions are based upon recognition of these trade-offs, which can be discovered as well as made quantitative using a spreadsheet to explore hand analysis. The spreadsheet is also an interface between hand analysis and PSPICE to aid verification of the assumptions of hand analysis, and to alert us to wrinkles that must be added to our thinking if we want reasonable designs.

Appendix: the diode-connected transistor

The small-signal equivalent circuit for Q_{Ref}, which has the collector shorted to the base (diode connection), is shown here to be a simple resistor, r_{REF}. This simple resistor replaces Q_{Ref} in the small-signal circuit of Figure 8. The small-signal circuit for Q_{Ref} is shown in Figure 26.

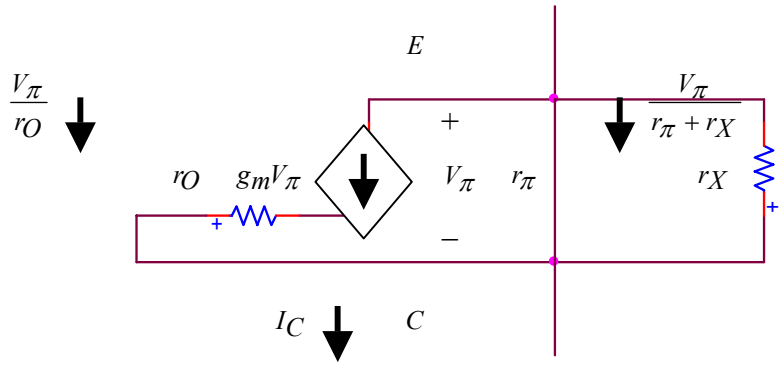

Figure 26
Small-signal circuit for reference transistor Q_{Ref}

Because the base and collector are short-circuited, base and collector are the same node. The voltage between collector and base is V_π, so the currents in the various branches are as shown in Figure 26. Consequently the total current flowing between collector and emitter is EQ. 25 below:

EQ. 25

$$I_C = \frac{V_\pi}{r_O} + \frac{V_\pi}{1/g_m} + \frac{V_\pi}{r_X + r_\pi} = \frac{V_\pi}{r_O /\!/ (1/g_m) /\!/ (r_X + r_\pi)}.$$

That is, the transistor behaves like a resistor of value r_{REF} given by EQ. 26:

EQ. 26

$$r_{REF} = r_O /\!/ (1/g_m) /\!/ (r_X + r_\pi).$$

Rewrite this resistance in terms of the current as shown in EQ. 27:

EQ. 27

$$\frac{1}{r_O /\!/ (1/g_m) /\!/ (r_X + r_\pi)} = \frac{1}{r_O} + g_m + \frac{1}{r_X + \frac{\beta_{AC}}{g_m}} = \frac{I_C}{V_{AF}} + \frac{I_C}{\eta_F V_{TH}} \left(1 + \frac{1}{\beta_{AC}} \frac{1}{1 + r_X / r_\pi}\right).$$

Because $V_{AF} >> V_{TH}$ (for example, for the Q2N2907A in Figure 1 at 27°C, V_{AF} = 115.7 V and $V_{TH} \approx 26$ mV), the last term dominates the sum, and to a very good approximation we can take the small-signal equivalent circuit of Q_{Ref} to be a single resistor of value r_{REF} given by EQ. 28:

EQ. 28

$$r_{REF} \approx \frac{1}{g_m}.$$

Exercises

1. Go through the chapter using an n-channel mirror with a simple model Q_nVAF using dot-model statement:

   .model Q_nVAF NPN (Bf={B_F} Is={I_S} Vaf={V_AF} Nf={N_F} Rb={r_X}),

   and instead of fitting the pnp Q2N2907A make the Q_nVAF match the PSPICE-provided npn Q2N2222 transistor.

2. Use the spreadsheet to make trade-off plots using I_C as the dependent variable and R_N and V_M as independent x-axes. Describe how you obtain these charts. Discuss the origins of trends in your charts.
3. Make a pnp mirror design using Q2N2907A transistors similar to the one in the chapter but for specifications of $R_N \geq 1$ MΩ for $V_A \leq 8$ V.

Answer: Using the spreadsheet calibrated for $I_C = 10$ mA, we find a design using GOAL SEEK for R_E =306.5 Ω and R_R = 1.983 kΩ with I_C = 4 mA. We check the β-values as shown in Figure 27 and the ideality coefficient as shown in Figure 28 and update the spreadsheet.

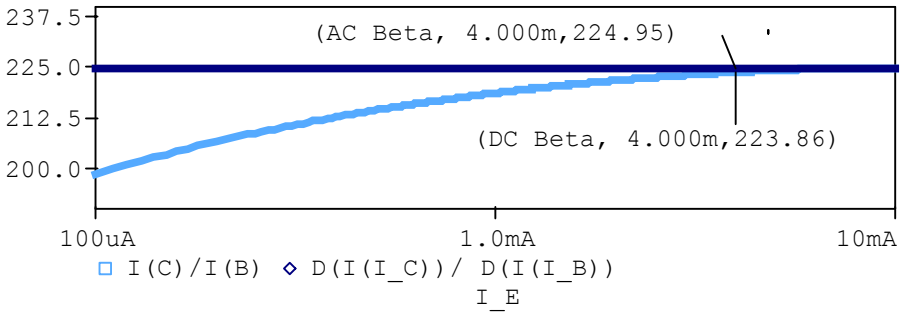

Figure 27

Check of β-values at initial guessed $I_C \approx 4$ mA

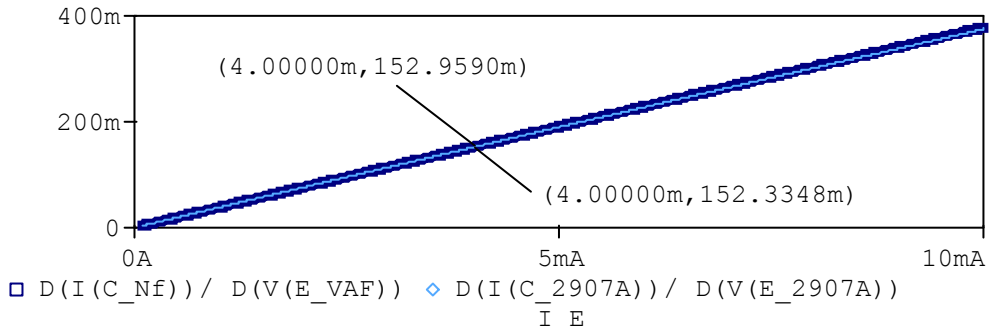

Figure 28

External g_m-values for use in finding new η = 1.0040976

We then use GOAL SEEK again to design to specification. See Figure 20. The new design is R_E = 305.7 Ω, R_R = 1971.8 Ω, I_C = 4.02 mA. These resistance values are put

into PSPICE to check the design. The PROBE output file is shown in Figure 29, and the Q-point in Figure 30.

NAME	Q_Q_Out	Q_Q_Ref
MODEL	Q2N2907A	Q2N2907A
IB	-1.80E-05	-1.80E-05
IC	-4.02E-03	-4.02E-03
VBE	-0.762	-0.762
VBC	0.00261	0
VCE	-0.765	-0.762
BETADC	224	224
GM	0.155	0.155
RPI	1460	1460
RX	10	10
RO	2.88E+04	2.88E+04
CBE	1.27E-10	1.27E-10
CBC	1.48E-11	1.48E-11
CJS	0.00E+00	0.00E+00
BETAAC	226	226
CBX/CBX2	0.00E+00	0.00E+00
FT/FT2	1.74E+08	1.74E+08

Figure 29
PROBE output file for design

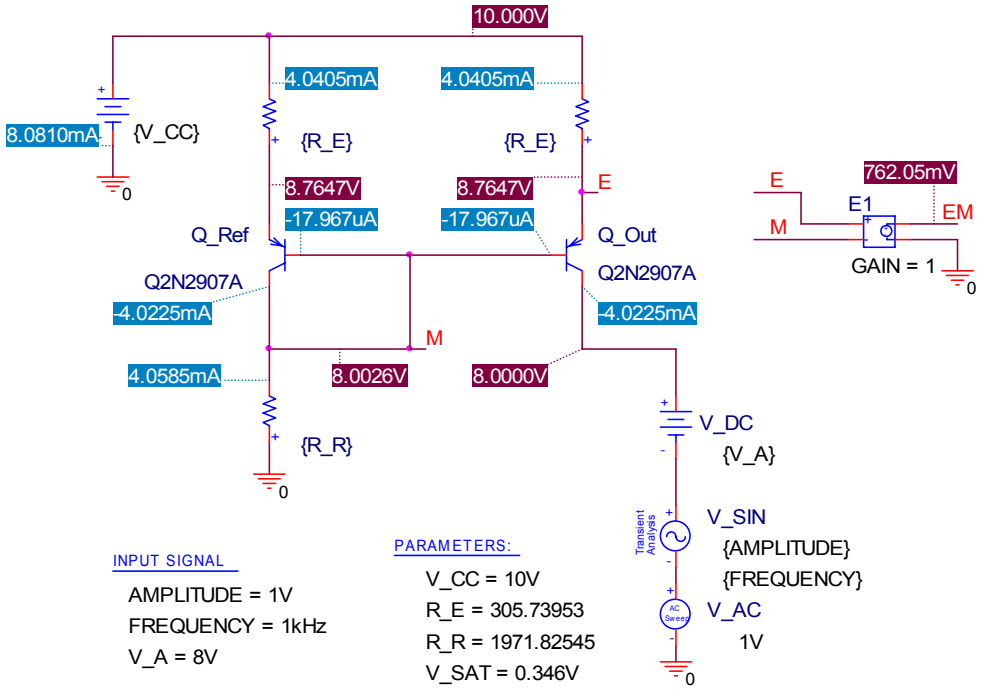

Figure 30
Q-point for V_A = 8 V

Figure 29 shows r_π = 1.46 kΩ, compare to the spreadsheet value 1.45 kΩ, r_O = 28.8 kΩ compared to 28.8 kΩ, good agreement. Figure 31 shows the mirror characteristics.

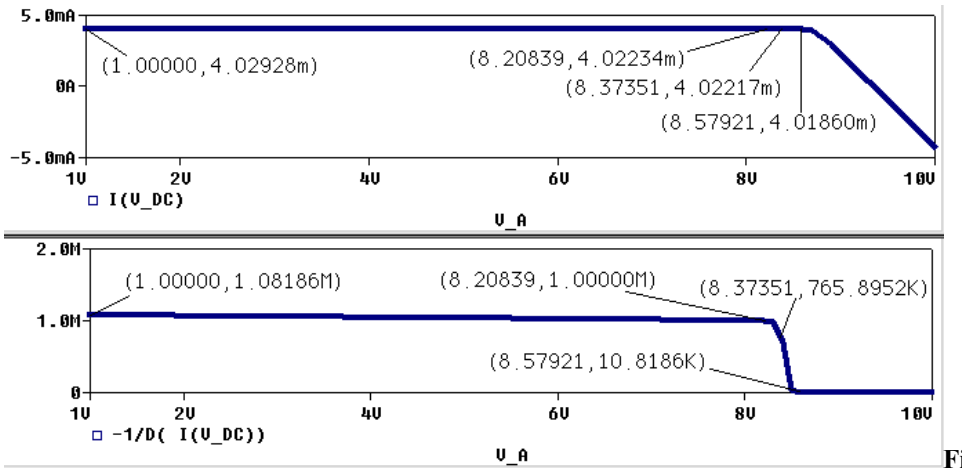

Figure 31 Mirror characteristics for design

The mirror satisfies $R_N \geq 1$ MΩ for $V_A \leq 8.2$ V, exceeding the 8V specification. The mirror provides only 4 mA of current however, compared to 12 mA for the design presented in the chapter.

Software elements presented

CAPTURE and PSPICE

Finding AC and DC betas (Figure 3)

Introduction to the pnp dot-model statement:

.model Q_pVAF PNP (Bf={B_F} Is={I_S} Vaf={V_AF} Nf={N_F} Rb={r_X})

Introduction to the pnp dot-model statement for the Q2N2907A transistor.

Dealing with base resistance r_X

Finding the ideality factor η to match a more realistic bipolar model (Figure 7)

Another example implementing a small-signal circuit (Figure 13)

EXCEL

Another example of implementing a hand analysis in the spreadsheet, verifying it and using it for design